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Transistor-level thermal management in wide and ultra-wide bandgap power semiconductor transistors: A review

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ABSTRACT

Power electronics are advancing in efficiency and power density, but high-frequency, miniaturization, and integration introduce novel thermal management challenges. Effective thermal management is crucial to maintaining the efficient operation of semiconductor transistors. As package-level thermal management approaches its heat dissipation limits, transistor-level thermal management near the junction can markedly enhance cooling efficiency, thereby increasing output power density and expanding safe operational margins. Most existing reviews concentrate on package-level thermal management, a comprehensive classification and in-depth comparison of transistor-level thermal management aimed at the more microscopic heat transfer process inside the device is limited. Therefore, by analyzing the self-heating mechanism of wide and ultra-wide bandgap power semiconductor transistor, this review paper summarizes the strategy of controlling junction temperature (T_j) from two aspects: junction-to-case thermal resistance ($R_{th,j\text{-}c}$) and power loss (P_{loss}). Firstly, different side-cooling methods are commented from the junction and bottom heat transfer paths. On this basis, a large number of complex micro/nano interface impediments to heat transfer are discussed, including the mechanism and modulation methods of interface heat transfer. Transistor design methods for optimizing internal electric field (E-field), specific on-resistance ($R_{on,sp}$), and switching characteristics are reviewed, which are feasible and effective for optimizing loss and preventing local hot spot generation. Lastly, we discuss the primary challenges in current strategic development and offer guidance for future advancements in transistor-level thermal management. These proven or unproven concepts hold the promise of extremely efficient thermal management, driving leaps forward in (U)WBG power electronics.

1. Introduction

Power electronics systems have made significant advancements in energy efficiency and power density [1,2]. However, as power devices continue to miniaturize, operate at higher frequencies, and integrate more densely, the self-heating effect and associated thermal management challenges have become increasingly prominent [3–5]. Inadequate heat dissipation can lead to junction temperatures (T_j) exceeding safe limits, which not only reduces device efficiency but may also lead to device failure, thereby compromising the long-term stability and reliability of the system [6]. Power semiconductor transistors are essential for achieving efficient energy conversion in power electronics

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systems. Consequently, effective thermal management strategies are critically needed to ensure stable and reliable operation under high-power conditions. Such strategies are vital for minimizing energy loss, reducing carbon dioxide emissions, and promoting the development of more sustainable technologies [7].

Over the past two decades, the emergence of wide band gap (WBG) power transistors, including vertical silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) and lateral gallium nitride high electron mobility transistors (GaN HEMTs), has marked a revolutionary leap in power electronics [8,9]. These WBG-based semiconductors exhibit exceptional electrical properties and robust thermal characteristics, such as high electron mobility and critical field strength. The next frontier in power electronics is anticipated to be led by ultra-wide band gap (UWBG) semiconductors like gallium oxide (Ga_2O_3), $Al_xGa_{1-x}N$, and diamond, which are poised as potential candidates for the next generation of advanced power technologies [10–15].

UWBG semiconductors, characterized by band gaps (E_g) greater than 4 eV, maintain higher critical fields (E_c) compared to traditional WBG electronics. This property enables them to achieve higher blocking voltages with lower $R_{on,sp}$ and smaller chip sizes [16,17]. Table .1 outlines the bandgap and thermal conductivity (k_T) values of various (U)WBG semiconductors. Despite their superior physical properties, (U)WBG electronics pose significant challenges in thermal management due to their extremely high-power densities compared to traditional silicon (Si) electronics. As power electronics, particularly (U)WBG devices, approach the heat dissipation limits imposed by maximum power consumption at the package-level, effective thermal management must evolve from conventional macroscopic approaches to targeted transistor-level strategies that address localized hot spots by prioritizing peak T_j reduction over average device temperature control. While traditional package-level thermal management relies on macroscopic techniques, such as heat sinks, thermal interface materials, and forced convection, to dissipate heat from the external casing to the ambient environment, these methods are fundamentally constrained by thermal spreading resistance and bulk material limitations, failing to mitigate sub-device thermal gradients and localized nanoscale extreme hotspots, which are critical failure mechanisms in high-power-density semiconductor devices. In contrast, transistor-level thermal management directly focus on microscopic pathways, targets heat generation and dissipation at the semiconductor junction through advanced materials, innovative structural designs, and dynamic power loss optimization, enabling precise heat extraction from active regions, which is a critical capability for (U)WBG devices operating at high-power-density. This paradigm shifts from package-centric to junction-centric thermal management underscores the necessity of integrating both macroscopic and microscopic approaches to fully realize the performance and reliability potential of next-generation power electronics.

Physical characteristics differ between vertical and lateral power transistors due to their distinct transistor architectures. By increasing the thickness of drift region without reducing the transistor size, vertical transistors can lower the $R_{on,sp}$ and increase the BV [18,19]. Vertical transistors exhibit more uniform heat distribution due to current flow through a larger cross-sectional area. In contrast, lateral transistors conduct current primarily through the surface, increasing the likelihood of local hot spot formation in the thin conductive channel near the surface [20]. Vertical transistors excel in high-power scenarios due to their superior power handling capacity and more straightforward thermal management [21]. SiC MOSFETs exemplify successful vertical power transistors, driving ongoing advancements in other emerging ultra-wide band gap (UWBG) vertical transistor technologies. Conversely, lateral transistors offer advantages for applications requiring high frequencies and low power. While lateral GaN HEMTs are relatively mature, they have spurred research into transistor-level thermal management due to their low k_T substrate and complex multi-layer thermal boundary resistance (TBR) [22]. Ga_2O_3 and $Al_xGa_{1-x}N$, as prominent UWBG semiconductors, are primarily investigated in lateral transistor configurations. These materials exhibit extremely low k_T, intensifying the self-heating effect and necessitating efficient heat dissipation strategies. Diamond stands out due to its exceptionally high k_T, offering significant potential for effective heat dissipation applications. Recent advances in transistor-level thermal management have significantly advanced the fundamental understanding of this critical field, as evidenced by several insightful reviews [6,23–26]. However, the rapid development of (U)WBG semiconductor technology has introduced new challenges in managing the intricate electro-thermal interactions spanning multiple scales. To address these emerging demands, this review introduces a comprehensive electro-thermal co-design framework that systematically unifies thermal resistance reduction with power loss optimization for effective T_j control in (U)WBG devices. Departing from conventional methodologies, our analysis offers: (1) A holistic evaluation of thermal management strategies across diverse heat transfer pathways; (2) A critical assessment of interfacial phonon scattering mechanisms and their role in thermal regulation; (3) Systematic connections between nanoscale thermal transport phenomena and device-level electrothermal performance. By integrating material insights with transistor design principles, this work offers transformative strategies that transcend traditional limitations of material-centric or package-focused thermal management in high-power electronics. The central objective of transistor-level thermal management outlined in this review is to reduce T_j starting with junction-to-case thermal resistance ($R_{th,j\text{-}c}$) and P_{loss}. Fig. 1 presents a comprehensive overview of the key strategies employed in transistor-level thermal management, including reducing $R_{th,j\text{-}c}$ through side-cooling and interface thermal transport, and optimizing P_{loss} through transistor design.

In reviewing techniques to reduce the $R_{th,j\text{-}c}$ of power transistors, various heat transfer paths and interfacial heat transfer mechanisms have been considered. Specific strategies are employed in each method to enhance the thermal performance of device. Top-side cooling focuses on enhancing direct heat transfer from the transistor junction to the package, thereby mitigating thermal limitations, such as the low k_T observed in materials like Ga_2O_3 [27]. Despite its effectiveness, top-side cooling may be constrained by the heat dissipation area of the electrode. Bottom-side cooling in power transistors leverages a substrate with high k_T or incorporates embedded microchannels to enhance heat dissipation. This approach capitalizes on the larger surface area of the substrate to efficiently dissipate heat generated within the transistor, thereby reducing the $R_{th,j\text{-}c}$ [28]. Combining both top-side and bottom-side cooling approaches, double-side cooling offers comprehensive thermal management. By integrating multiple heat transfer paths, this method optimizes heat dissipation across the entire transistor structure [29–31]. The transistor is a complex structure composed of multiple layers, including semiconductors, metals, and dielectric materials. Within this structure, interface heat transport plays a significant role in determining the $R_{th,j\text{-}c}$. TBR or thermal boundary conductivity (TBC), which are inversely related, are commonly utilized to denote the heat transfer capacity at the interface between different materials or layers within a transistor. High TBR values create bottlenecks in interfacial heat transfer, thereby limiting the overall heat dissipation efficiency and potentially compromising the performance and reliability of transistors. Therefore, enhancing interface heat transport and minimizing TBR are critical scientific and technical challenges in the field of power transistor heat dissipation. As another focus of transistor-level thermal management, transistor design has a major impact on both electrical

Table 1
Physical properties of silicon (Si) and major (U) WBG semiconductors. (x = 0.3–0.7 for $Al_xGa_{1-x}N$). Data were adopted from Refs. [9–15].

Property	Si	SiC	GaN	Ga_2O_3	$Al_xGa_{1-x}N$	Diamond
E_g (eV)	1.12	3.3	3.45	4.8	3.4–6	5.5
k_T (W/m K)	150	370	130	11–27	8.8–9.7	2400

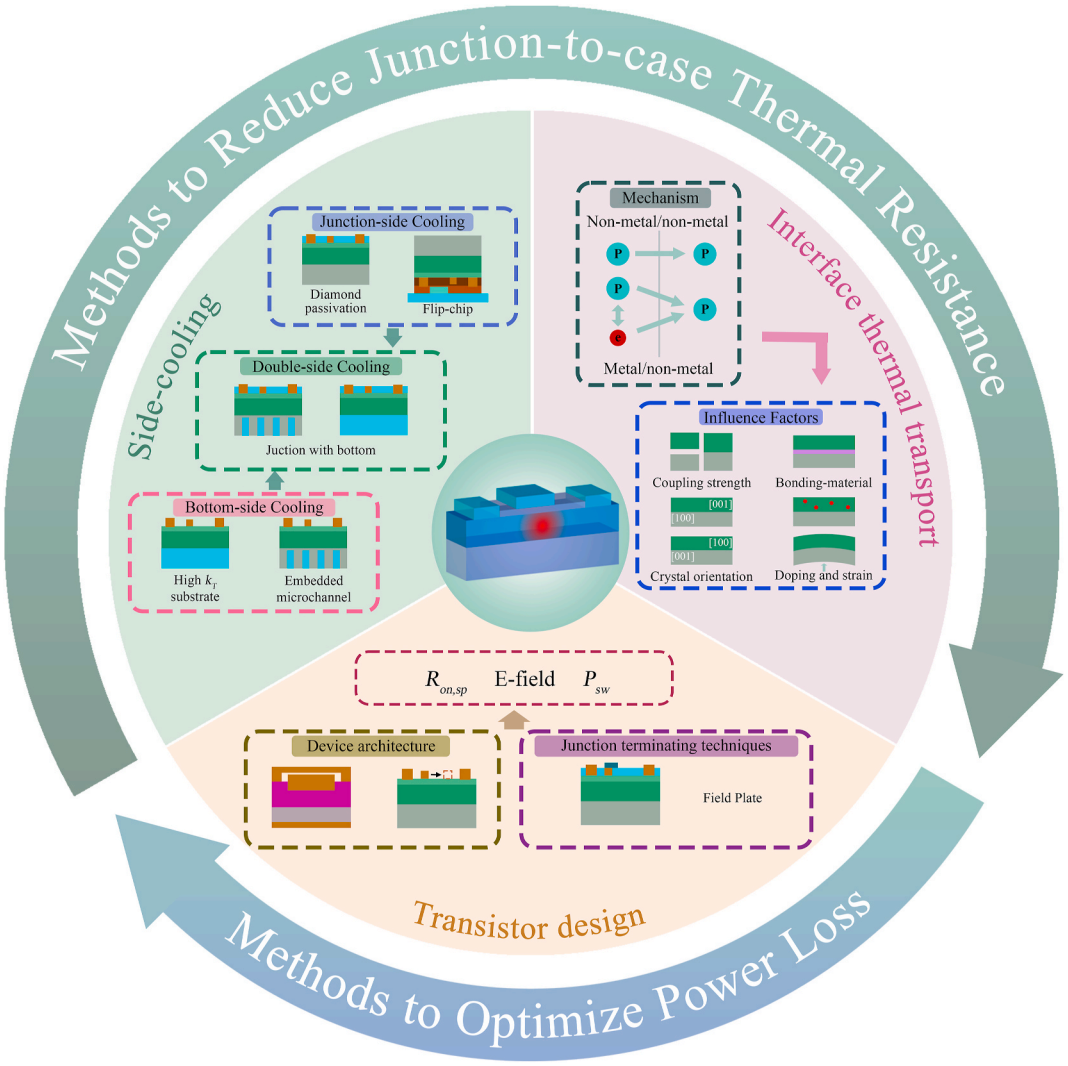

Fig. 1. Schematic of transistor-level thermal management in (U)WBG power semiconductor transistors.

performance and thermal management [32]. P_{loss} is minimized through transistor design, consequently leading to a significant reduction in heat generation. Optimizing of the P_{loss} can be achieved by reducing $R_{on,sp}$, alleviating E-field congestion and improving switching characteristics through improved transistor design. To achieve thermo-electric co-design, it is crucial to ensure that thermal management does not compromise the essential performance of the power transistor.

This review focuses on the transistor-level thermal management of (U)WBG power semiconductor transistors. The present situation and challenges of transistor-level thermal management are analyzed from the perspective of $R_{th,j\text{-}c\ c}$ and P_{loss}. The article is structured as follows: section.2 analyzes the self-heating mechanism and thermal resistance (R_{th}) network of typical power transistors; section 3 reviews the methods and research status of side-cooling; section 4 discusses the mechanism and modulation methods of interface thermal transport; section 5 reviews the current research status of transistor design as a method for transistor-level thermal management; section 6 discusses the existing challenge and future prospects of transistor-level thermal management of (U)WBG electronics; section 7 provides a summary of the article.

2. Thermal analysis of power semiconductor transistors

With the ongoing advancement in electronic devices, the power density continues to increase, leading to local heat flux densities of 1 kW/cm^2 or higher, thereby elevating local temperatures [33,34]. This phenomenon significantly impacts the performance and operational reliability of electronic devices. In the absence of efficient thermal management techniques, the self-heating of electronic devices intensifies. (U)WBG electronics feature larger bandgaps, which help mitigate uncontrolled carrier conduction induced by elevated thermal energy. However, higher T_j can compromise ohmic and gate contacts [23]. Moreover, severe internal overheating diminishes charge carrier mobility, thereby reducing output power and increasing gate leakage current [35–37]. Therefore, to meet the demands of high-power density environments, implementing advanced thermal management techniques is imperative. The primary objective of effective thermal management strategies is to comprehend the underlying physical mechanisms of (U)WBG self-heating. Fig. 2 illustrates the fundamental transistor structures of a vertical SiC MOSFET [38], a lateral GaN HEMT [39], a lateral Ga_2O_3 MOSFET [40], and the R_{th} network of power transistors.

In Fig. 2 (a), the typical SiC MOSFET utilizes a PN junction formed by a doped P-base region and a lightly doped N-drift region to block voltage. When the channel opens, electrons flow through the JFET region created between the two P-base regions into the drift region [41,42]. The peak T_j is consistently observed in the JFET region of planar gate MOSFETs, located beneath the gate oxide layer [43]. Research into vertical power transistors based on other (U)WBG semiconductors is actively pursued to fulfill the demands of high voltage (>1 kV) and high current (>100 A) applications [44,45].

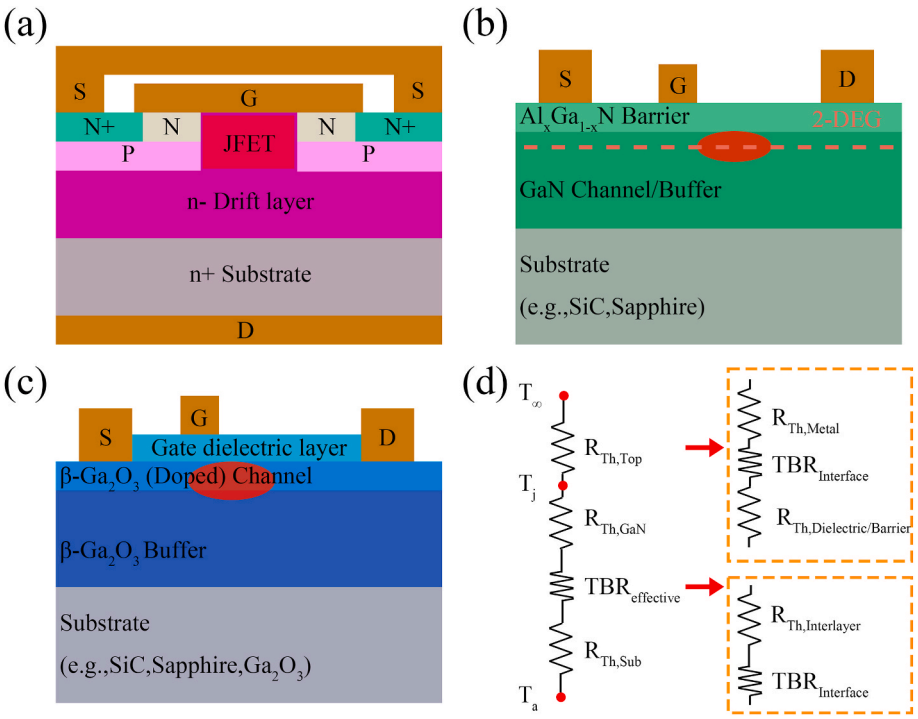

Fig. 2. Schematic of (a) a SiC MOSFET, (b) a GaN HEMT, (c) a β-Ga_2O_3 MOSFET and (d) R_{th} network of power transistors.

Recent research in emerging semiconductors has prominently featured lateral transistors, with GaN HEMTs being among the most well-developed. A traditional GaN HEMT typically comprises a substrate, GaN buffer, and AlGaN barrier, as depicted in Fig. 2 (b). Control of the channel switch is achieved through modulation of the gate voltage. The polarization effect at the interface between the GaN buffer and the AlGaN barrier induces a high concentration of two-dimensional electron gas (2DEG). The hot spots in the 2DEG channel become more concentrated while bringing high current density [46–48]. Ga_2O_3 MOSFETs share a structural similarity with GaN HEMTs, but they incorporate a metal oxide insulator (dielectric layer) separating the source and drain. To establish ohmic contact between the electrode and the semiconductor, heavily doped N-type regions are positioned beneath the source and drain. These regions exhibit significantly higher electron concentrations compared to surrounding areas [49]. The peak T_j occurs in the submicron region near the gate drain edge channel, where a Ga_2O_3 MOSFET experiences highly localized power consumption and heating during transistor operation [50,51].

Determining the primary factors influencing T_j is crucial for devising effective thermal management strategies. The following formula can be employed to calculate T_j for a power transistor operating at room temperature (T_a):

$$T_j = (R_{th,j-c} + R_{th,c-a})P_{loss} + T_a \tag{1}$$

where $R_{th,c\text{-}a}$ is the thermal resistance of the case to the ambient, which can be optimized by advanced packaging technology. Analyzing the formula, effective measures for transistor-level thermal management involve reducing $R_{th,j\text{-}c}$ and optimize P_{loss} under certain T_a and packaging process.

Based on the R_{th} network model in Fig. 2 (d), heat transfer occurs via two main thermal pathways. The $R_{th,j\text{-}c}$ primarily encompasses the semiconductor material, substrate material, metal electrodes and their intricate interfaces. Effectively reducing $R_{th,j\text{-}c}$ requires focused efforts on two key aspects: side-cooling and enhancing interface thermal transport. Currently, widely used low-cost substrates such as Si and sapphire constrain the performance enhancement of (U)WBG transistors due to their low k_T [52]. For Ga_2O_3, despite its advantages in terms of UWBG and economic benefits from melt growth techniques [53,54], its exceptionally low k_T exacerbates self-heating effects. Additionally, the complexity of interfaces and strong phonon boundary scattering significantly contribute to high TBR, thereby impeding efficient heat transfer [55–60].

P_{loss} is another critical factor affecting T_j, which can be considered as the total power loss ($P_{t,loss}$) and the local power loss (power loss per unit volume, $P_{v,loss}$). For unipolar transistors, the total power loss ($P_{t,loss}$) is the sum of conduction loss (P_{con}) and switching loss (P_{sw}) [3,61]:

$$P_{t,loss} = P_{con} + P_{sw} = DR_{on,sp}\frac{I_0^2}{A} + fk_sA \tag{2}$$

where D is the duty cycle, A is the chip area, I_0 is the conducting current, f is the switching frequency, k_s is a circuit-related switching parameter. In the process of electronic miniaturization and high frequency, $R_{on,sp}$ and switching characteristic plays a direct role in $P_{t,loss}$. Lowering the $R_{on,sp}$ and improving the switching characteristics effectively reduce the $P_{t,loss}$ of the transistor through specific transistor design optimizations [62].

When a voltage is applied to a vertical transistor, the E-field distributes evenly throughout the transistor, unlike in lateral transistors where E-field spikes can occur at the gate edge [63,64]. This characteristic contributes to vertical transistors having a more uniform heat distribution compared to lateral transistors, as a uniform thermal field is often associated with a uniform E-field distribution. During current flow between the source and drain, the carrier density is very high. Collision energy loss between electrons and the lattice results in self-heating [65–67]. The energy transferred by electrons to the lattice is composed of [67]:

$$P_{v,loss} = nev_d(E)E \tag{3}$$

where n is the electron density, e is the charge of the electron, and $v_d(E)$ is the field dependent drift velocity [68], and E is the E-field intensity. Therefore, the uniform E-field helps prevent local high-power density caused by peak E-field spikes and mitigates the formation of extreme hot spots. Designing transistors with strategies aimed at dispersing charge

density can further alleviate hot spots associated with E-field accumulation [3]. By implementing appropriate design measures, engineers can achieve more uniform E-field and heat distribution within the transistor [69,70]. In summary, transistor-level thermal management necessitates integrating thermal considerations into the transistor design from the outset of its development process. This proactive approach ensures that thermal effects are effectively managed, thereby enhancing the overall performance, reliability, and longevity of electronic devices.

3. Side-cooling in transistor-level thermal management

During the operation of a power transistor, the heat generated in the active region disperses outward through two primary paths: from the top (junction) and from the bottom. Integrating high k_T materials on both sides of the power transistor can effectively reduce the $R_{th,j\text{-}c}$, thereby inhibiting heat accumulation. In addition, in areas with strong operability, such as the substrate region, introducing liquid to promote heat exchange with the active region of the transistor represents a proactive approach to heat dissipation. This section will explore side cooling strategies in transistor-level thermal management, encompassing junction-side cooling, bottom-side cooling and double-side cooling.

3.1. Junction-side cooling

Given that hot spots in power transistors typically manifest closer to the transistor junction, effective heat extraction from the top of the transistor becomes crucial. Junction-side cooling methods rely on layers above the channel, such as AlGaN, passivation materials, and gate insulators, rather than the costly substrate material. Junction-side cooling generally encompasses three primary approaches: diamond passivation, two-dimensional (2D) material radiator, and flip-chip integration.

3.1.1. Diamond passivation

Due to the high k_T and excellent insulating properties of diamond materials, integrating diamond as a passivation layer atop the transistor can significantly improve the thermal dissipation of hotspots to the surface, thereby reducing T_j. Diamond passivation emerged as a pioneering method validated initially on GaN HEMTs, showcasing its competitiveness in thermal management applications. However, the bond between diamond and GaN is inherently weak and lacks a feasible covalent Ga-C bond. A notable challenge encountered in the direct growth of diamond on GaN using CVD arises from the weak interface and the thermal expansion coefficient disparity between these two materials. Specifically, GaN exhibits a higher thermal expansion coefficient at room temperature (5.59×10^{-6} K^{-1}) compared to diamond (4.38×10^{-6} K^{-1}). This difference results in considerable stress and strain at the interface during temperature variations, which can potentially lead to structural damage or delamination. Cuenca et al. [71] conducted research on the thermal stress of CVD diamond films integrated with GaN, as shown in Fig. 3 (a). During the heating phase, internal stresses within the diamond film cause deformation, influencing the final structure upon subsequent cooling to room temperature. The researchers suggest that prestressing the film before growth could potentially mitigate these thermal stresses and improve the integrity of the diamond-GaN interface. Building upon these findings, Arivazhagan et al. [72] proposed a new structure in where the PCD layer is selectively deposited on the drain rather than directly on the transistor channel. Technology Computer Aided Design (TCAD) analysis demonstrated that this approach, compared to traditional GaN-on-Si HEMTs, reduces self-heating effects and enhances saturated drain current. Fig. 3 (b) depicts a method of seeding diamond with both micro- and nano-seeds proposed by Soleimanzadeh et al. [73]. This approach offers improved crystallinity, larger grain size, and superior interface coverage compared to conventional nano-seeding methods. Consequently, it achieves a

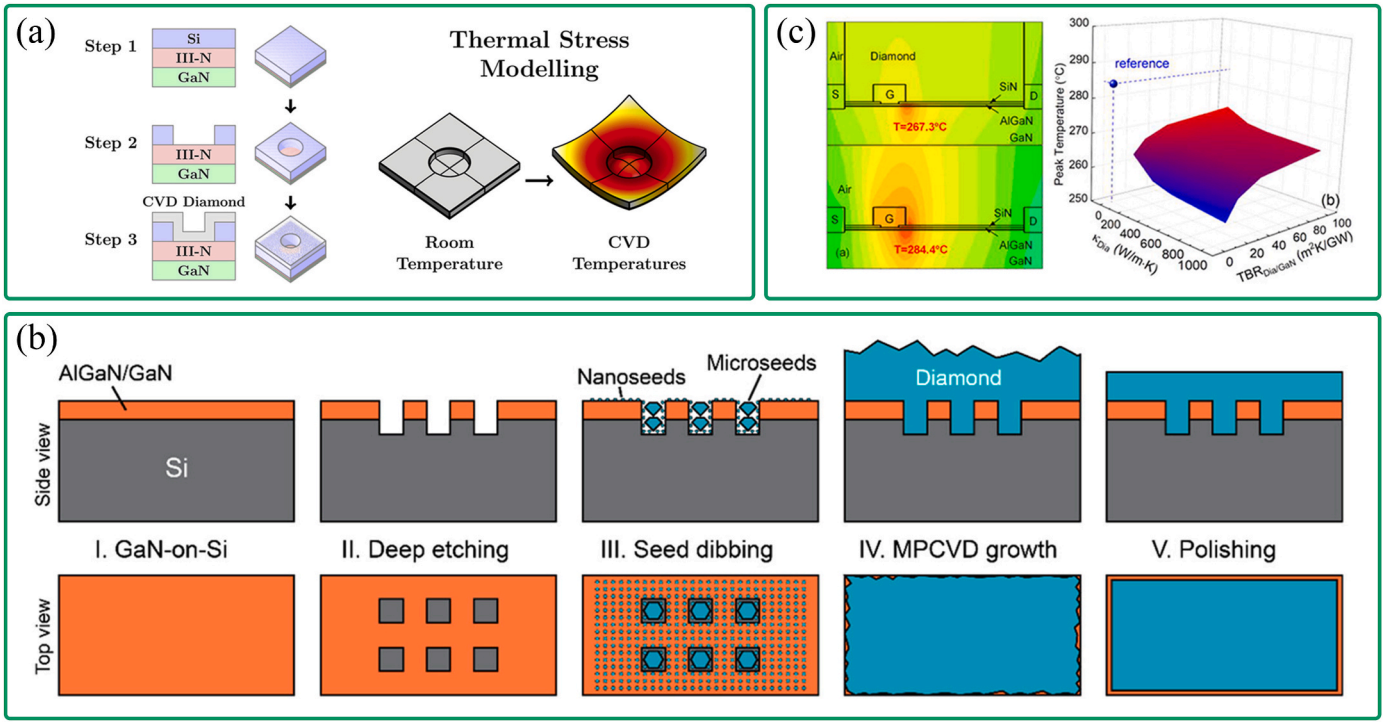

Fig. 3. (a) Approaches to diamond on GaN/III-N integration using membrane fabrication. The GaN/III-N membrane numerical model of the displacement field in micrometres (z scale 10 for visibility) at the beginning of microwave plasma assisted CVD growth [71]. (b) Schematic diagram of diamond-on-GaN substrate fabrication using the seed dibbling method: (I) GaN-on-Si substrate, (II) deep etching of holes, (III) seed dibbling using both nano- and microseeds of diamond, (IV) microwave plasma chemical vapor deposition (MPCVD) diamond growth, and (V) diamond polishing (*Copyright © 2021, American Chemical Society*) [73]. (c) The thermal distribution of devices with and without a diamond heat spreader across the active region at a power density of 15 W/mm (left); The peak temperature of the device as a function of the k_T of diamond and the TBR between diamond and GaN (right) [74].

two-fold increase in k_T of GaN-on-Si with just a 20 μm thick diamond layer. Wu et al. [74] studied the effect of diamond thermal conductive sheet on the actual thermal performance of the device, and simulated the device using the thermal properties extracted by time-domain thermal reflection (TDTR). Fig. 3 (c) illustrates the thermal distribution of devices with and without a diamond heat spreader, revealing a temperature difference of 17.1 °C between the two methods. Hao et al. [75] deposited a smooth nano-diamond film with high thermal conductivity on the GaN surface. The high crystallinity of the NCD film results in a low TBR (12.8 ± 0.64 m^2 K/GW) and high thermal conductivity (200 ± 40 W $m^{-1}K^{-1}$) for the entire NCD layer. Notably, when the thickness of the top diamond film is restricted, the improvement of TBR has more significant effect on the heat transfer at the top than the improvement of diamond k_T. The issue of TBR will be discussed in section.4.

The superior thermal performance of PCD passivation layers has been successfully demonstrated in GaN transistors, prompting interest in its application to Ga_2O_3 transistors as well. Given the low k_T of Ga_2O_3, the effectiveness of PCD passivation layers becomes particularly critical for managing heat dissipation during high-frequency operations. Yuan et al. [31] demonstrated the effectiveness of employing a high k_T (400 W/K) film on top of a β-Ga_2O_3 transistor through thermal simulations. The rapid extraction and transfer of heat to the source and drain metals can reduce the maximum T_j by 26 %. Malakoutian et al. [76] achieved successful growth of PCD on β-Ga_2O_3 using CVD for the first time. The PCD/β-Ga_2O_3 interface was smooth, with the β-Ga_2O_3 substrate remaining undamaged. They measured the TBR of the PCD/β-Ga_2O_3 interface to be 30.2 ± 1.8 m^2 K GW^{-1}, representing a significant advancement in junction-side cooling strategies for β-Ga_2O_3 electronic transistors. The impact of the PCD passivation layer thickness on the channel temperature was investigated by Kim et al. [77]. For the PCD passivation layer at 267 nm thick, the effect of TBR on the temperature rise of the channel was negligible. However, for 1 μm and 2 μm thick PCD layers, the steady-state temperature rise varied by approximately 8 % and 18 %, respectively, across different TBR values. In a recent work, nanocrystal diamond (NCD) deposited via microwave plasma enhanced chemical vapor deposition (MP-CVD) by Masten et al. [78] as a Junction-side cooling solution for lateral β-Ga_2O_3 transistors. The addition of NCD thermal diffusion layer reduces the total gate thermal resistance of heterogeneous FET by 42 %. Generally, achieving high interface quality and employing mechanical-based methods to reduce TBR at the diamond passivation layer interface are crucial for maximizing heat dissipation advantages [79].

3.1.2. 2D material radiator

Coupled radiators play a pivotal role in high-power semiconductor electronics by significantly expanding the heat exchange area, thereby enhancing heat dissipation efficiency. The 2D structure and large surface to volume ratio of graphene make it and its related 2D materials ideal for heat dissipation [80,81]. Balandin et al. [82] pioneered the application of graphene-based heat spreaders for cooling GaN HEMTs. Fig. 4 (a) illustrates the concept of using graphene-graphene as a top surface heat spreader. In Fig. 4 (b), simulations depict the temperature distribution with and without a graphene-based heat spreader in AlGaN/GaN HEMTs, demonstrating a potential reduction of approximately 20 °C in hot spot temperatures for transistors operating at around 13 W/mm. This approach introduces a novel category of materials for localized heat propagation, maintaining superior thermal properties at the nanoscale and representing a revolutionary advancement in thermal management

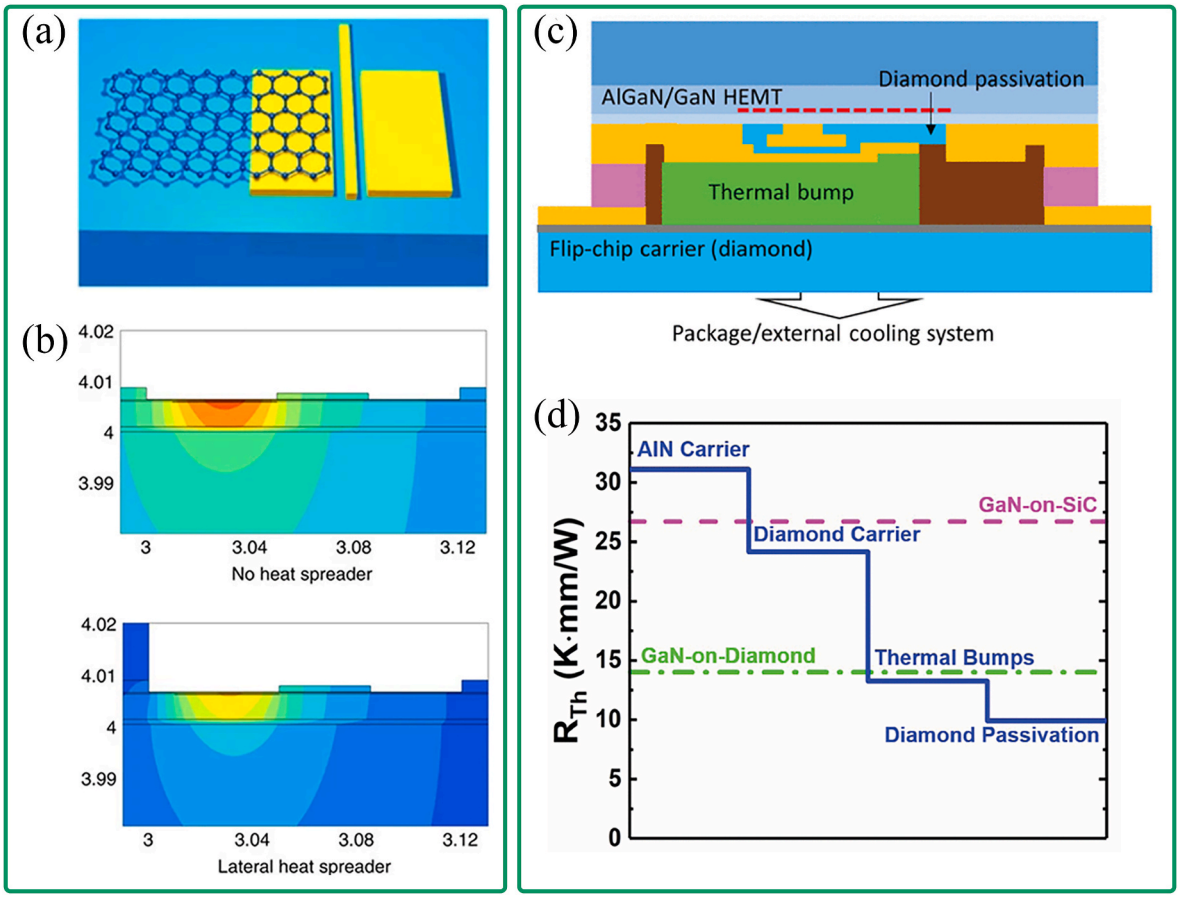

Fig. 4. (a) Schematic of the graphene-based heat heat spreaders attached to the drain contact of the AlGaN/GaN HEMT. (b) Temperature distribution in AlGaN/GaN HFET without (top) and with (bottom) the heat spreader [82]· (c) Thermally optimized diamond-incorporated flip-chips configuration. (d) Thermal optimization process of the flip-chip integration scheme (*Copyright © 2021, IEEE*) [91].

strategies. Subsequently, researchers employed Au/Pt/Ti micro coil test structures to evaluate the effectiveness of graphene as a heat spreader [83–85], highlighting its capability for efficient heat dissipation. However, the zero-band gap of graphene necessitates passivation through SiO_2 (a low k_T material) between hot spots, which partially impedes heat transfer. Hexagonal boron nitride (hBN), another 2D material with thermal properties akin to graphene, can act as a 2D insulating heat spreader in direct contact with hot spots [86–88]. Choi et al. [86] found that a 35 nm thick layer of h-BN on a glass substrate was sufficient to reduce the hot spot temperature by 4.1 times. Nazim et al. [87,88], in their studies using Au/Pt/Ti micro-coil test structures, investigated the heat dissipation capabilities of h-BN. They concluded that a multilayer h-BN, approximately 2 nm thick, is optimal and sufficient for effective heat dissipation through direct contact. Due to their outstanding properties, 2D materials hold significant promise for enhancing heat dissipation in power electronics, offering prospects for integration into future applications in power electronics.

3.1.3. Flip-chip integration

Flip-chip integration represents a competitive method for junction-side cooling, proven to significantly reduce transistor $R_{th,j\text{-}c}$ to manageable levels [89–91]. Lundh et al. flip-chip integrated AlGaN on sapphire onto a diamond carrier [89], achieving a remarkable 78 % reduction in $R_{th,j\text{-}c}$ through the use of gold thermal bumps. In flip-chip configurations, the thermal bump is typically positioned between the transistor and the carrier wafer to enhance heat extraction from the top. Chatterjee et al. [90] used simulations to demonstrate that incorporating a 2 μm × 100 μm thermal bump above the channel region adjacent to the gate in β-$(Al_xGa_{1\text{-}x})_2O_3/Ga_2O_3$ FETs could further reduce ΔT_j by an additional 12 %. Carriers play a crucial role in facilitating effective flip-chip integration strategies. Shoemaker et al. [91] investigated the use of PCD as a carrier for integrated flip-chip cooling of GaN HEMTs, as shown in Fig. 4 (c). Fig. 4 (d) illustrated the thermal optimization process of the flip-chip integration scheme. By adopting PCD carriers, they achieved a 22 % reduction in $R_{th,j\text{-}c}$ compared to AlN carriers, resulting in approximately 24.15 K mm/W. Through further optimization involving thermal bumps, they achieved a 45.1 % reduction (~13.25 K mm/W) in $R_{th,j\text{-}c}$, and an additional 25 % reduction (~9.87 K mm/W) through diamond passivation. This optimized transistor configuration exhibits lower $R_{th,j\text{-}c}$ than current state-of-the-art GaN-on-diamond HEMTs. In the heat transfer process from the semiconductor material to the metal electrode, TBR between the metal electrode and the semiconductor material plays a significant role [92–94], influencing overall heat transfer efficiency. Additionally, the dielectric layer separating the gate electrode from the channel impacts thermal management, making high-quality and high k_T dielectric materials preferable [95].

Furthermore, when selecting gate materials for (U)WBG power devices, several critical factors beyond high k_T must be carefully considered: low leakage, low $R_{on,sp}$, high BV, environmental stability, and high crystallization temperature. Optimizing these factors in gate material selection for (U)WBG power devices is critical for achieving high efficiency, reliability, and performance across various applications, including power electronics and high-power applications.

3.2. Bottom-side cooling

Bottom-side cooling is a thermal management technique designed to enhance heat dissipation by transferring heat through the substrate to the package-level heat sink. Leveraging the extensive area beneath the transistor, bottom-side cooling offers significant advantages in heat dissipation compared to top-side cooling. Strategies such as high k_T substrates and embedded microchannels are widely adopted and have demonstrated effectiveness in improving the thermal performance of transistors. Notably, achieving optimal performance in the combination between a chip and its substrate requires careful co-design considerations for mechanical bonding, electrical bonding, and thermal bonding. These aspects are crucial for ensuring effective interface thermal conduction, electrical conduction, and mechanical adhesion simultaneously. These approaches have garnered considerable interest among researchers in recent years.

3.2.1. High k_T substrate

Recently, researchers have been actively pursuing high-conductivity materials to replace conventional substrates in electronic systems for improved cooling efficiency [96–98]. Fig. 5 (a) and (b) compare the k_T, Debye temperature, and coefficient of thermal expansion of various semiconductor materials alongside high k_T substrate materials. When choosing a substrate, prioritizing k_T is essential. Moreover, minimizing the TBR is facilitated by selecting materials with closely matched Debye temperatures and coefficients of thermal expansion between the semiconductor and substrate materials. This approach maximizes the benefits derived from high k_T. Materials such as SiC, diamond, boron arsenide (BAs), and other high k_T materials have emerged prominently in this pursuit, prompting extensive theoretical and experimental research efforts [99–103].

SiC: SiC stands out as a well-established semiconductor material known for its high k_T, making it highly suitable for use as a substrate material. The relatively minimal lattice mismatch between GaN and SiC results in low dislocation density, rendering GaN epitaxy on SiC particularly attractive [104–106]. Binari et al. [104] were the first to successfully grow AlGaN/GaN HEMT on SiC substrates. Through the continuous efforts of scientists, Feng et al. [105] developed a high-quality GaN film buffer layer with low TBR on SiC, utilizing an ultrathin AlGaN buffer layer with low aluminum content. This ultra-thin buffer layer enhances crystal quality and diminishes TBR at the GaN/SiC interface. Similar cooling techniques employed for GaN can also be applied in Ga_2O_3-based transistors, where heat dissipation requirements are more critical. In 2019, Xu et al. [107] achieved the pioneering heterogeneous integration of 2-inch β-Ga_2O_3 films on 4H-SiC and Si (001) substrates by an ion cutting process. Compared with reported Ga_2O_3-on-Ga_2O_3 transistors, Ga_2O_3-on-SiC transistors exhibit excellent thermal stability at operating temperatures up to 500 K, attributed to the high k_T of the SiC substrate. In related work by the same group, Schottky barrier diodes (SBD) were prepared on β-Ga_2O_3/SiC heterostructure material [108], exhibiting a 25 % lower temperature rise at equivalent power levels compared to β-Ga_2O_3 wafers alone. Song et al. [109] reported the fabrication of Ga_2O_3/4H-SiC composite wafers through a fusion bonding method, as shown in Fig. 6 (a), achieving successful growth of the Ga_2O_3 epitaxial layer on the composite substrate. In a subsequent work [110], the same group proposed low-temperature growth axial Ga_2O_3 transistors (Fig. 6 (b)), with high thermal performance and the highest power (~300 MW cm^{-2}) reported to date among heterogeneous integrated Ga_2O_3 transistors. As illustrated in Fig. 6 (c), due to the enhanced heat transfer performance of the composite substrate, the ΔT_j of the transistor operating at a power density of 2.63 W/mm (L_{GD} = 55 μm) is 2.4 times lower than that of the Ga_2O_3 substrate. Furthermore, the thermal performance of the multi-finger device is examined. Due to thermal cross-talk between adjacent current channels, self-heating is notably intensified. In Fig. 6 (d), a substantial reduction in channel temperature of approximately 8 times is observed in the ideal multi-finger configuration, suggesting potential to lower device R_{th} below that of current commercial GaN-on-SiC transistors. Recently, Xu et al. [111] used ion cutting and surface-activated bonding techniques to integrate β-Ga_2O_3 heterogeneous onto SiC substrates. Combined with thermal modeling, the thermal resistance of Ga_2O_3-on-SiC devices is two orders of magnitude lower than that of Ga_2O_3-on- Ga_2O_3 devices. In addition, the research group [112] found that compared with the epitaxial Ga_2O_3 MOSFETs, the I_{on}/I_{off} degradation of Ga_2O_3-SiC MOSFETs was reduced by 1.5 orders of magnitude, indicating great thermal stability. Through additional device packaging, the thermal resistance of Ga_2O_3-SiC MOSFETs reached a record low of 4.45 K mm/W.

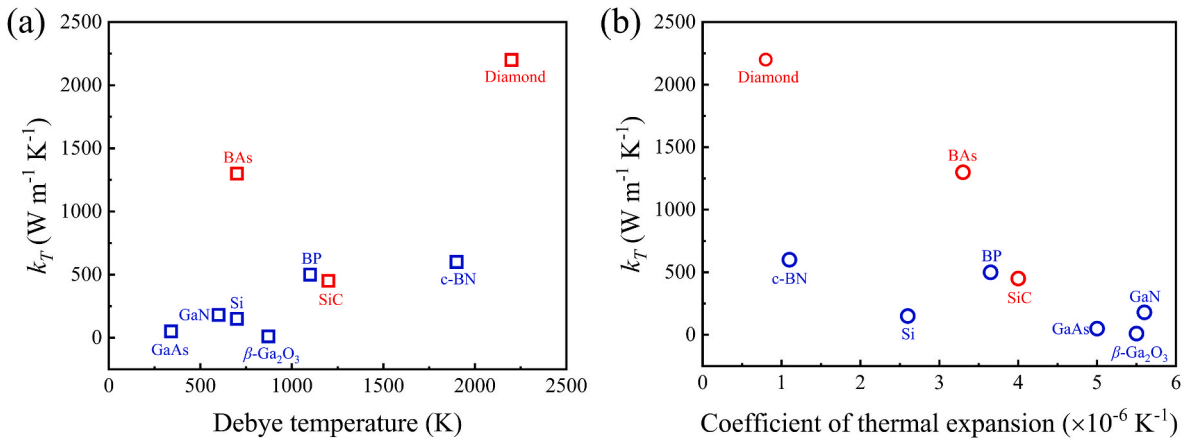

Fig. 5. (a) Room-temperature k_T and Debye temperatures of representative semiconductors and high k_T materials. (b) Room-temperature k_T and coefficient of thermal expansion of representative semiconductors and high k_T materials.

Diamond: To further mitigate the thermal limiting effect of power transistors, the integration of power transistors with high k_T diamond shows great potential [113]. Diamond is currently the leading research prototype high k_T material for high-performance power electronics cooling. Integrating diamond with semiconductors offers substantial potential to improve heat dissipation capabilities. Chernykh et al. [114] deposited PCD film on a thin functional silicon layer of 'silicon-o-n-insulator' (SOI) wafer, followed by the growth of a GaN-based heterogeneous structure. This approach mitigates the detrimental effects of high PCD growth temperatures on GaN layer performance. Compared to conventional GaN-on-SiC based HEMTs, the method reduces surface temperatures by more than 50 °C and increases mean time to failure by 2 orders of magnitude. Recently, Kagawa et al. [115] demonstrated the successful transfer of AlGaN/GaN/3C-SiC layers grown on Si to large-size diamond substrates and subsequently fabricated GaN HEMTs on diamond. The transfer and fabrication process of the GaN/3C-SiC/diamond HEMTs using the bonding-first concept is shown in Fig. 6 (e). Remarkably, even after annealing at 1100 °C, no shedding of the 3C-SiC/diamond bonding interface was observed, highlighting its critical role in enabling high-quality GaN crystal growth on diamond substrates. Fig. 6 (f) and (g) illustrate the temperature distribution and the temperature rise with power dissipation (P_{diss}) of the GaN HEMTs on the Si, SiC, and diamond. Compared to other structures, GaN-on-diamond exhibits significantly lower T_j, demonstrating clear thermal superiority. Furthermore, diamond substrates, initially proven effective for GaN applications, have shown promise in the realm of β-Ga_2O_3 as well. Oh et al. [116] utilized thermal simulation to demonstrate that diamond substrates reduced the lattice temperature of β-Ga_2O_3, consequently mitigating drain current degradation. Matsumae et al. [117] combined the surface functionalized β-Ga_2O_3 with the PCD substrate directly in the atmosphere at 250 °C. The interface structure analysis confirmed atomic-level bonding between the β-Ga_2O_3 and diamond surfaces, devoid of nanoholes, cracks, or intermediate layers. Recently, Kim et al. employed finite element modeling [118] to analyze the thermal properties of transistors using diamond substrates and submicron-thin β-Ga_2O_3 layers. The thermal model of the transistor is depicted in Fig. 6 (h). At a T_j limit of 200 °C, the β-Ga_2O_3 transistor can handle a maximum power density of up to 8.6 W/mm. Gu et al. [119] fabricated Ga_2O_3/diamond heterojunctions by the atomic layer deposition (ALD) method, and measured the k_T of Ga_2O_3 thin films and the TBC of Ga_2O_3/diamond by TDTR to be 5.13 W/(m·K) and 19.22 MW/(m^2·K). Lately, Hu et al. [120] designed and realized the fabrication of GaN devices on diamond-SiC composite substrates. Compared with GaN-on-SiC technology when the base temperature is T_{base} = 25 °C and P_{diss} = 7.2 W/mm, the surface temperature of the improved cooling structure is reduced by 52.5 °C and the thermal resistance is reduced by about 41 %. The epitaxial growth of Ga_2O_3 films on diamond substrate is an active area of research [121–123], with expectations for significant advancements. However, the large lattice mismatch and thermal mismatch between diamond and Ga_2O_3 are responsible for the poor TBR, thereby diminishing the advantages of inherently high k_T in diamond.

BAs: BAs boasts an impressive isotropic thermal conductivity of 1300 W m^{-1} K^{-1} [101], coupled with mechanical and thermophysical properties that are highly compatible with power semiconductors. The integration and characterization of BAs with other semiconductor materials are crucial for its potential application in thermal management strategies. Kang et al. [124] achieved a significant milestone by integrating a BAs-cooled substrate with a GaN device, demonstrating experimental measurements of an operational AlGaN/GaN HEMT (Fig. 6 (i)). Fig. 6 (j) assesses the impact of TBR and demonstrates that diamond exhibits a slight advantage in scenarios where TBR (dotted lines) is not included in the simulation. However, upon including TBR in the simulation (dashed lines), it becomes evident that BAs achieves significantly lower hot spot temperatures compared to diamond. Research findings confirm the superior cooling efficiency of BAs, revealing a lower hot spot temperature (~60 K) compared to diamond (~110 K) and SiC (~140 K) under equivalent transistor power densities, as shown in Fig. 6 (k). This enhanced thermal management capability of BAs is attributed to its unique phonon band structure and effective interface matching. Currently, BAs has been limited to laboratory-scale manufacturing and testing due to challenges such as non-uniformity and frequent defects. Within the same BAs sample, the k_T can vary significantly, ranging from less than 500 to more than 1200 W m^{-1} K^{-1} [125]. Improving the quality of grown BAs crystals and developing practical, cost-effective manufacturing processes are critical objectives.

Researchers have explored substrate screening methods suitable for different semiconductor devices. Fahdi et al. [126] used machine learning methods to search for promising substrates or radiators to cool β-Ga_2O_3 devices. These descriptors based on the primitive cells of substrates are easy to calculate after structural optimization, providing a new way to quickly screen potential substrates from large-scale material pools. In addition, etched microchannel structures filled with high k_T materials are also an alternative thermal management method [127, 128].

3.2.2. *Embedded microchannel*

In addition to the high k_T substrate, the integration of embedded microchannel cooling in close proximity to hot spots represents a more promising and efficient thermal management approach [129–132]. Embedded microchannels actively dissipate heat by introducing coolant directly into the transistor's active region, thereby significantly

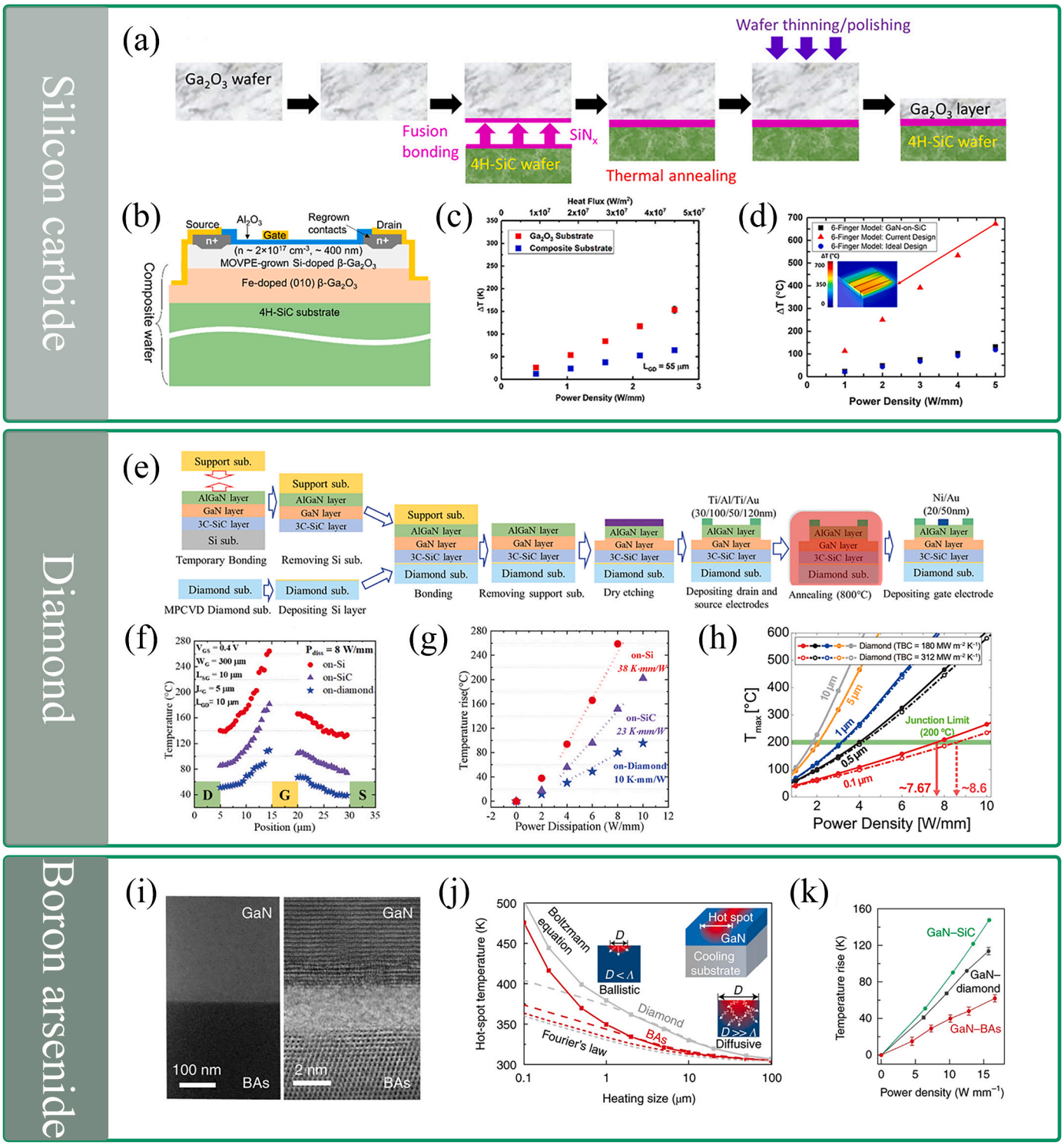

Fig. 6. (a) Wafer-bonding and -thinning approach used to create the Ga_2O_3 composite (*Copyright © 2021, American Chemical Society*) [109]. (b) Cross-sectional schematic of a Ga_2O_3 MOSFET fabricated on the composite. (c) Comparison of the temperature rise of the real and ideal 6-finger devices. (d) Steady-state channel temperature rise of the MOSFETs fabricated on the composite substrate and a bulk Ga_2O_3 wafer with $L_{GD} = 55$ μm (*Copyright © 2023, American Chemical Society*) [110]. (e) The transfer and fabrication process of the GaN/3C-SiC/diamond HEMTs using the bonding-first concept. (f) The temperature distribution of the GaN HEMTs on the Si, SiC, and diamond at P_{diss} 8 W/mm. (g) The relationships between the temperature rise of the gate edge and P_{diss} for the GaN HEMTs on the Si, SiC, and diamond [115]. (h) Maximum transistor temperature and power density for single-gate Ga_2O_3 transistors [118]. (i) Cross-sectional SEM (left) and high-resolution TEM (right) images of a GaN–BAs structure, revealing the atomically resolved interface. (j) Simulations of the hot-spot temperatures for the two best thermal conductors (BAs and diamond), as a function of heating size (from 100 μm to 100 nm). (k) A plot depicting GaN temperature versus power density, measured via Raman spectroscopy at the drain side, 0.5 μm laterally from the T-gate edge [124].

mitigating the self-heating effect. Vertical transistors feature an additional drift layer alongside the channel layer and substrate, allowing for BV scaling by adjusting the thickness of the drift layer without increasing the transistor's footprint [133,134]. This characteristic provides a larger surface area near the drift region, facilitating their application in thermal management strategies [95]. Vadimirova et al. [135] proposed integrating a microchannel cooler within the drift region as a potential solution for vertical power transistors. A number of fluids through-holes perpendicular to the PN junction of the transistor are designed in the drift region. According to their findings from electrical simulations, the electrical performance of the transistor would not be negatively affected. Building upon this foundation, Dede et al. [136] proposed three concepts of embedded cooling for vertical WBG semiconductor transistors, as shown in Fig. 7 (a). These concepts are as follows: A) embedding microchannels directly into the substrate of the power transistor; B) embedding microchannels into the lower electrode of the transistor; Or C) connecting a vertical power transistor to a silicon-cooled chip with microchannels and through silicon via (TSV) via an intermediate metallization plus thermal interface material (TIM) layer. Concept A demonstrates superior heat dissipation performance due to the etched microchannels in the substrate. However, this approach may potentially impact the electrical performance of the transistor by increasing the $R_{on,sp}$; Concept B circumvents potential electrical performance issues, yet the deposition/attachment of a thick metal layer and the micromachining required to incorporate microchannels into the lower electrodes pose significant challenges. Concept C utilizes existing Si micro-electro-mechanical systems (MEMS) devices and TSV fabrication techniques. This concept introduces additional TIM and potentially increases the R_{th}. Jung et al. [137] conducted a detailed exploration of Concept A using one-dimensional thermal fluid modeling. The analysis showed that the temperature of the WBG transistor can be maintained below 200 °C even under a high heat flux of 1 kW/cm^2. However, achieving low pressure drop in both single-phase and two-phase flows remains challenging due to restrictions imposed by the

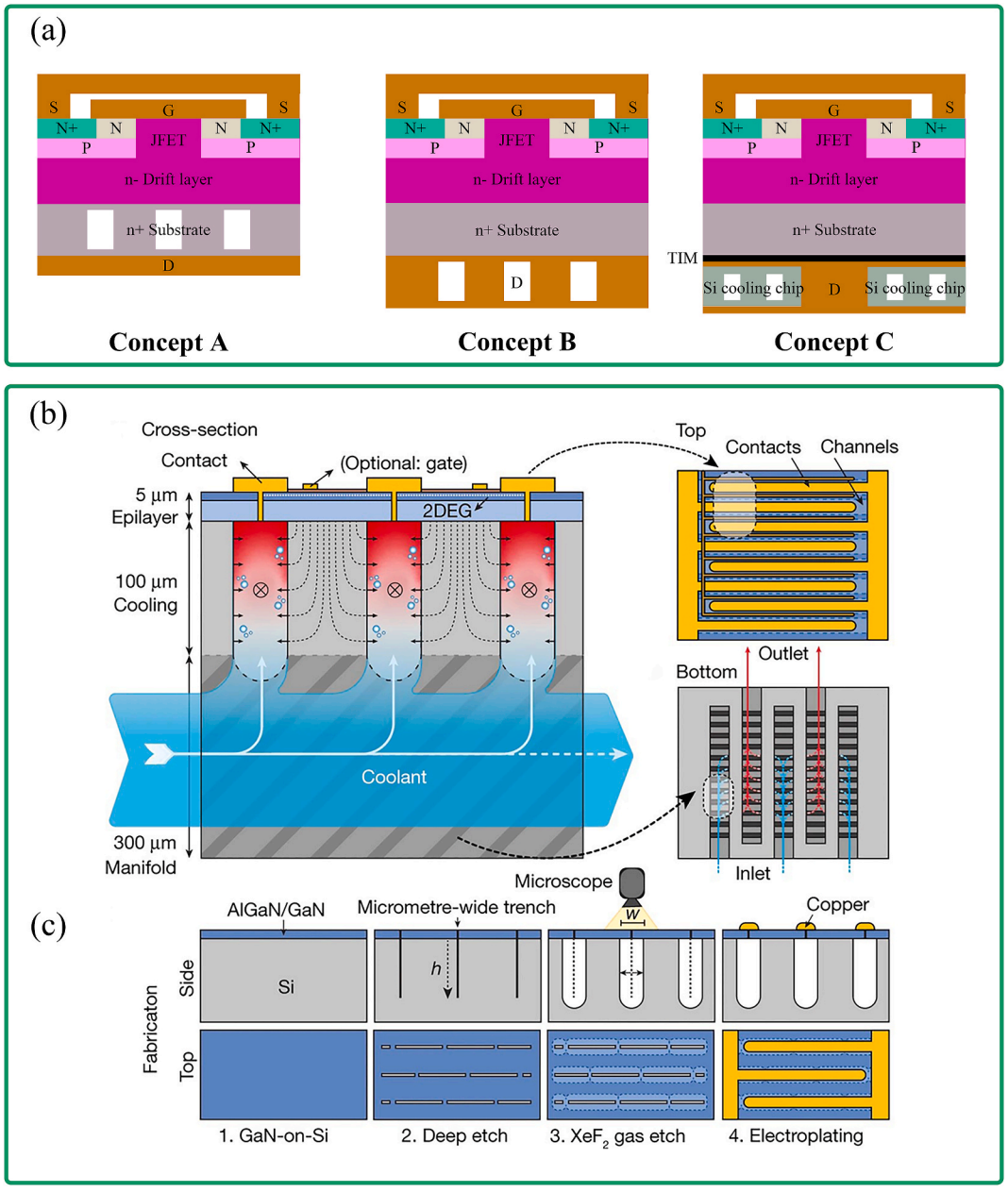

Fig. 7. (a) Three concepts for embedded cooling of vertical current WBG semiconductor transistors. Concepts are taken from Ref. [136]. (b) The schematic of the microchannels. (c) The fabrication process of the microchannels [139].

channel height in this embedded cooling technique. On the other hand, the Concept C was thoroughly examined by Zhou et al. [138] using a new jet impact chip cooling structure. A heat flow of up to 1 kW/cm^2 can be achieved at a temperature below 177.1 °C on average.

For lateral transistors, researchers have primarily explored embedded microchannels targeting the substrate region as an effective method for heat dissipation in GaN transistors [139–144]. Van Erp et al. [139] proposed a monolithically integrated manifold microchannel (mMMC) heat spreader, as shown in Fig. 7 (b). This innovative method enables the extraction of heat flux exceeding 1.7 kW/cm^2 with a minimal pumping power of 0.57 W/cm^2. Additionally, it predicts that the average additional energy cost for data center cooling could drop below 0.01 percent. Multilayer printed circuit boards (PCBs) are employed to direct coolant into microchannels embedded within semiconductor transistors, ensuring a fully integrated and aligned approach with the electronics to optimize heat dissipation. Fig. 7 (c) illustrates the fabrication process of the microchannels, commencing with anisotropic deep etching through a narrow incision in the AlGaN/GaN film to achieve the required microchannel depth. Subsequent isotropic gas etching completes the formation of the microchannels, thereby integrating transistor design and heat sink fabrication within a unified process. Recently, Nela et al. [140] integrated embedded liquid cooling on a 650 V, 50 mΩ GaN-on-Si commercial power transistor, demonstrating that embedded liquid cooling has no negative effect on the electrical performance of the transistor. Lian et al. [141] developed a design featuring a high-resistivity silicon (HR Si) interlayer embedded with four microchannels, each with dimensions of 30 μm width and 30 μm spacing. They achieved an average heat dissipation density of 5 kW/cm^2 in the active zone of GaN HEMT using deionized water as the cooling agent at a flow rate of 3 mL/min. Ye et al. [142] embedded the microchannels into the SiC substrate, achieving a gate heat flux of 6349.2 W/mm^2 at a coolant flow rate of 70 mL/min, representing a 1172 % increase compared to traditional remote cooling methods. Zhang et al. [143] proposed an embedded manifold microchannel cooling (EMMC) device, which obtained a high heat transfer coefficient of 105 W/(m^2 K). Lu et al. [144] established a R_{th} model for embedded HEMT microchannel cooling and observed a reduction of 50 °C in maximum gate temperature and a 43.14 % decrease in $R_{th,j\text{-}c}$ compared to remote cooling methods. The embedded microchannel cooling method has been shown to work well for AlGaN/GaN HEMTs and is expected to shed light on emerging semiconductor materials such as Ga_2O_3 microchannel cooling. Shuvro et al. [145] pioneered the use of infrared laser etching to embed microchannels in β-Ga_2O_3 substrates for cooling purposes. When the water flow speed is 50 ml/min and the input power of 3.5 W, the surface temperature can be reduced from ~140 °C to ~72 °C. This study offers valuable practical insights into embedded cooling techniques for Ga_2O_3 transistors.

In recent years, research on embedded microchannels has seen significant growth [146–149]. Despite this progress, achieving maximum compactness and highest thermal performance remains a challenge. A primary challenge in the development of next-generation (U)WBG power transistors lies in fabricating microchannels under ultra-thin conditions, typically less than 250 μm. Advancements in etching techniques tailored for UWBG materials [150–155] show promise in addressing this challenge. These techniques are crucial for enabling the fabrication of efficient microchannels in such thin substrates. Looking forward, embedded microchannel cooling is expected to emerge as a highly promising active cooling method [150,156] for future semiconductor devices. Continued research and development in this area will likely lead to enhanced thermal management solutions for high-power electronics.

3.3. Double-side cooling

Combining junction-side and bottom-side cooling methods through double-sided cooling presents a robust approach to maximize heat dissipation efficiency in semiconductor devices. Numerical simulations have shown that double-sided cooling of β-Ga_2O_3 transistors can effectively reduce the $R_{th,j\text{-}c}$ to as low as approximately 8.5 mm K/W, which is anticipated to be lower than that achieved with GaN-on-diamond structures [31,91]. In the study of Kim et al. [157], the R_{th} of the 10 μm thick β-Ga_2O_3 drift layer accounted for 90 % of the total $R_{th,j\text{-}c}$ of the transistor. The high R_{th} of β-Ga_2O_3 prevents the heat flow to the bottom, thereby diminishing the cooling effectiveness of costly high k_T materials like diamond (1000–2000 W/m·K) compared to more common materials such as Cu, AlN, or AlSiC (300–550 W/m·K). Therefore, focusing on enhancing heat dissipation from the junction-side is deemed more effective. Addition of junction-side cooling significantly reduces the maximum temperature of the transistor channel. Compared with bottom cooling, employing double-side cooling reduces the temperature by approximately 50 % for each additional convective heat transfer coefficient value.

Montgomery et al. [95] conducted simulations to assess the impact of junction-side cooling versus double-side cooling on the heat dissipation of β-Ga_2O_3 vertical transistors. Double-side cooling is slightly more efficient than top-side cooling (decreasing from 135 °C to 134 °C at 15 MW cm^{-2}), leading to the conclusion that even with double-sided cooling, the majority of heat dissipation still occurs through the top due to the relatively low k_T of the β-Ga_2O_3 material. Similarly, Chatterjee et al. [90] investigated double-side cooling in a flip-chip integration scheme using a Ga_2O_3/4H-SiC composite wafer and arrived at a comparable conclusion. Fig. 8 (a) illustrates the schematic diagram of the double-side cooling scheme. For double-side cooling,ΔT_j is only reduced 5 % compared to flip-chip designs. The enhanced double-side cooling design was shown to be able to handle a power density of about 9.5 W/mm at a T_j limit of 200 °C, as shown in Fig. 8 (b). Kim et al. [74] added a diamond passivation layer on β-Ga_2O_3-on-diamond for the best heat dissipation performance. The steady-state temperature rise was reduced by approximately 75 % compared to the baseline β-Ga_2O_3 MOSFETs, while also improving transient thermal performance. Notably, configurations with thicker diamond layers on top and thinner β-Ga_2O_3 layers exhibited the lowest temperature rise. For applications involving extreme temperatures or high-power densities, (U)WBG transistors, particularly Ga_2O_3 power transistors, benefit significantly from combined thermal management strategies such as double-side cooling to ensure stable operation.

4. Interface thermal transport in transistor-level thermal management

In Section 3, we discuss various heterogeneous integrated transistor-level thermal management methods. In practical heterogeneous integrated devices, numerous complex micro-nano interfaces impede the heat transport process [158]. Interface thermal transport plays an important role in near-junction heat transport. Due to the acoustic mismatch between the materials, heat carriers encounter difficulties in smoothly transferring across these interfaces, especially in micro- and nano-scale devices. TBR can even be an order of magnitude larger than the inherent R_{th} of the materials, often becoming a dominant factor impeding heat transport near the junction. In the context of GaN transistors on foreign substrates, TBR has been demonstrated to significantly contribute to the increase of T_j [159–161]. Given the diverse interface types and intricate energy transfer mechanisms involved in semiconductor transistors, TBR emerges as a central focus in thermal transport research [162,163]. This section examines issues related to interface heat transport in transistor-level thermal management, covering aspects such as interface thermal transport mechanism and influence factors.

4.1. Thermal transport mechanism

Interface atoms differ significantly from bulk atoms primarily

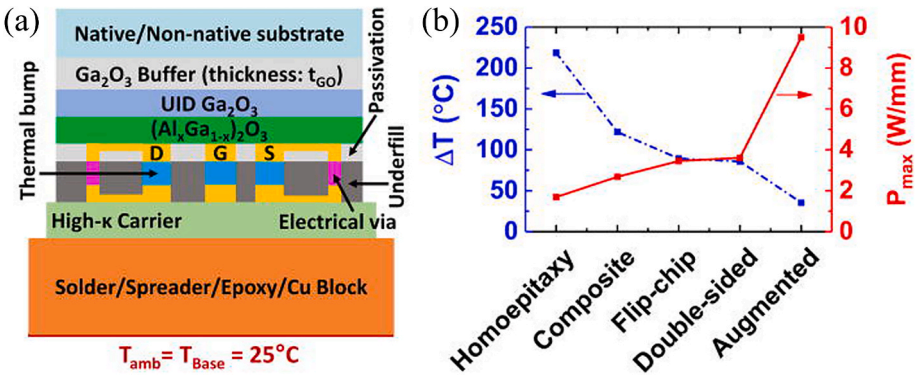

Fig. 8. (a). Schematic of the double-sided cooling scheme. (b) ΔT and the maximum power handling capability (P_{max}) for the different thermal management schemes [90].

because the local environment at the interface, including interatomic interactions and lattice structures, deviates from that of the bulk region [162]. Achieving a regular and orderly arrangement of local atomic structures at the interface is challenging due to lattice parameter mismatches, atomic misalignments, and different atomic bonding [164]. Additionally, interfaces composed of different materials or phases of the same material exhibit distinct energy states for thermal carriers (such as electron bands and phonon dispersion) on both sides [165]. Overall, understanding and controlling the atomic structure, interatomic interactions, and energy states at interfaces are crucial for optimizing thermal management in semiconductor devices. Addressing these interface-related challenges is essential for improving heat dissipation and overall device performance.

As depicted in Fig. 9 (a), during the process of energy transfer involving heat carriers across the interface, partial transmission and partial reflection back could occur. The disorder of the atomic structure and the mismatch in energy states lead to a significant temperature jump observed at the interface, which fundamentally constitutes TBR, as shown in Fig. 9 (b). The heat in the solid is mainly carried by various carriers such as electrons, phonons, magnetons, and 3He quasi particles in different forms of condensed matter. The research focus of this review centers on power transistors, particularly emphasizing the interfaces

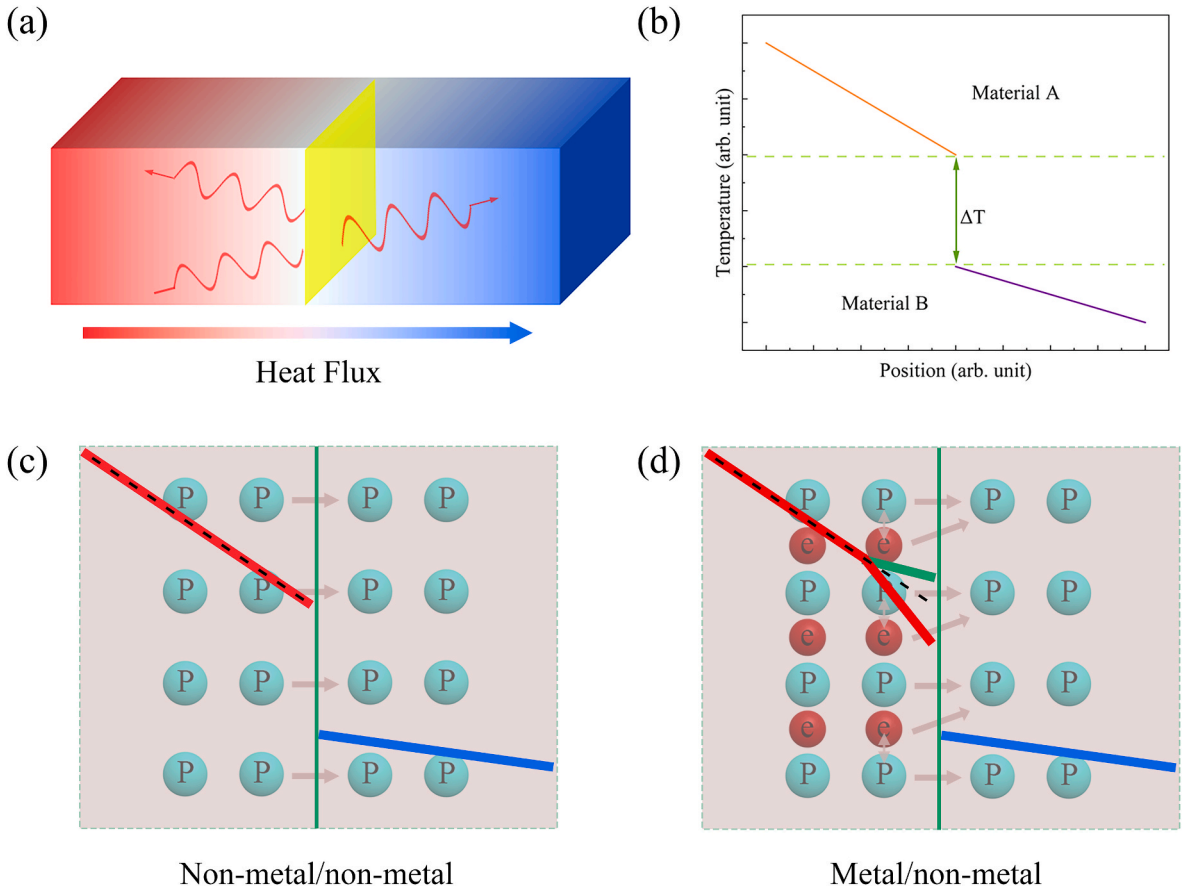

Fig. 9. (a) Schematic of phonon transport showing mode-specific transmission and reflection probability at the interface. (b) The steady state of temperature profile for interface. Schematic of heat carrier transmission at (c) Non-metal/non-metal interface and (d) Metal/non-metal interface. The dotted line represents fitting temperature (T_{fit}), the red line represents phonon temperature (T_{ph}), the blue line represents cooling temperature (T_c), and the green line represents electron temperature (T_e). (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

crucial to their operation. These interfaces include the dielectric/semiconductor interface, substrate/semiconductor interface, and metal/semiconductor interface, which have been identified as prominent research areas [162,166]. Based on the types of heat carriers involved, these interfaces can be classified into two main categories: non-metallic/non-metallic and metal/non-metallic interfaces, as shown in Fig. 9(c) and (d).

Non-metal/non-metal: For non-metal/non-metal interfaces, phonons serve as the primary carriers of heat, depicted in the accompanying Fig. 9 (c). Studies investigating the thermal properties of these interfaces, where phonons dominate heat transfer, typically employ models such as the acoustic mismatch model (AMM) and diffuse mismatch model (DMM) [167–169]. Detailed explanations of AMM and DMM, along with other associated research methodologies, exceed the scope of this review. Ma and Li et al. [170,171] utilized the AMM and DMM models to analyze the thermal transport characteristics at interfaces between Ga_2O_3 and various substrate materials. Ma et al. [170] demonstrated that the difference in TBC between various interfaces arises primarily from impedance mismatch and variations in phonon density of states (PDOS). The higher TBC observed at the Ga_2O_3/SiC interface compared to the Ga_2O_3/SiO_2 interface primarily stems from the significantly greater transmission function at the Ga_2O_3/SiC interface in contrast to the Ga_2O_3/SiO_2 interface. Li et al. [171] analyzed the heat transport mechanism at the interface in detail, focusing on PDOS and phonon participation ratios (PPR). Figure.10 (a) presents the simulated TBC, while Figure.10 (b) illustrates the overlap energy between materials at different interface regions. Their findings indicate that increased overlap energy enhances phonon heat transfer, thereby boosting PPR at the interface and influencing phonon-phonon interactions. AMM and DMM were developed on the basis of continuum theory, which ignored the detailed atomic structure of materials, thereby limiting their ability to accurately predict TBR or TBC in many cases. In contrast, several numerical methods account for the actual atomic structure of interfaces, such as the lattice dynamics method, atomic green function method, molecular dynamics (MD) simulation, Boltzmann transport equation and Monte Carlo method. Among them,

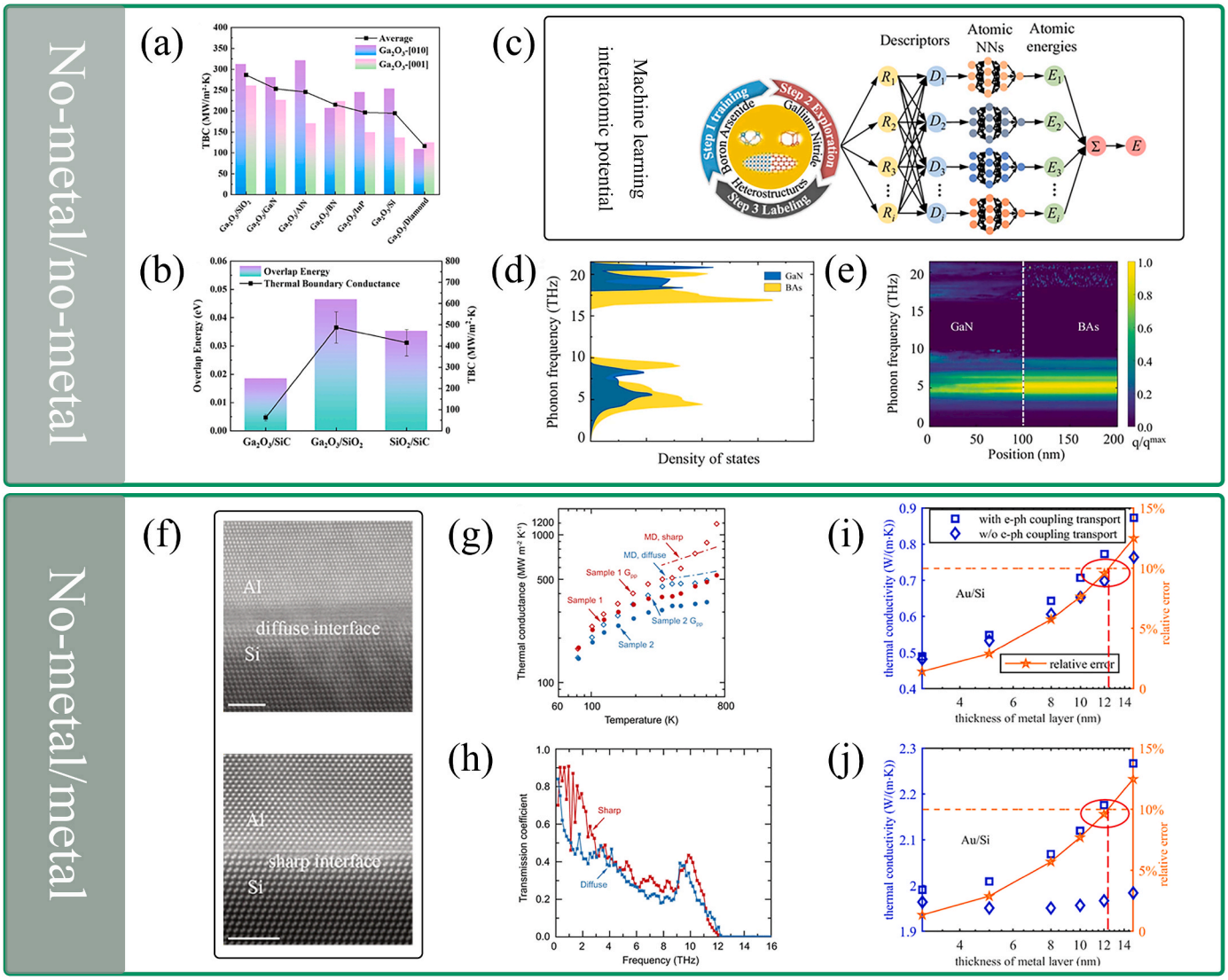

Fig. 10. (a) TBC for interface between Ga_2O_3 and different substrates, the colorful bars are TBCs along [010] and [001] directions, and the black spots are the average values of them. (b) Relationship between TBC and overlap energy of different interface areas [171]. (c) The basic steps of the MLIP. (d) The comparison of phonon density of states between BAs and GaN. (e) The spectral heat flux in GaN-BAs heterostructures, where the dash line indicates the interface and the color indicates the normalized density of heat flux [173]. (f) Cross-sectional TEM image of Al/Si with diffuse interface (top) and sharp interface (bottom). Scale bars are 2.5 nm. (g) Calculated thermal conductance of sharp (red dashed line) and diffuse (blue dashed line) Al/Si interfaces. (h) Phonon transmission coefficient for sharp (red) and diffuse (blue) interfaces [179]. Overall thermal conductivity of metal/semiconductor bilayer films of Au/Si by keeping thickness of Si layer at (i) 10 nm and (j) 50 nm [180]. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

MD simulation is particularly prominent as it offers a comprehensive in-situ approach to investigate interface phenomena in nanomaterials without these limitations.MD simulation rely on precise atomic potentials, which have been significantly enhanced in recent years by the emergence of machine learning interatomic potentials (MLIP) [172–175]. Wu et al. [173] employed neural network potentials (NNP) to develop precise and efficient MLIP of GaN/BAs. Figure.10 (c) outlines the fundamental steps of MLIP. They conducted multi-scale simulations of GaN/BAs heterogeneous structures, achieving an ultra-high TBC of 260 MW m^{-2} K^{-1}, closely matching experimental findings. The PDOS for GaN and BAs, along with the heat flux at the heterostructure interface, were calculated, as shown in Fig. 10(d) and (e). The extensive overlap in the PDOS suggests a strong correspondence in lattice vibrations between GaN and BAs, indicating favorable matching. Moreover, the interface exhibits a well-matched low-frequency heat flux, further underscoring the compatibility between these materials at the atomic level. The analysis shows that the underlying mechanism is rooted in the harmonious lattice vibrations of BAs and GaN. Sun et al. [175] utilized NeuroEvolution Potential (NEP) to construct a MLIP for β-Ga_2O_3/diamond heterogeneous structure with high accuracy. Their study highlighted the influence of state vibration density and interface structure on TBR at the interface. The utilization of MLIP effectively connects simulation outcomes with experimental findings, thereby encouraging further investigation into the mechanisms governing interfacial heat transfer.

Metal/non-metal: For metal/non-metal interfaces, where heat conduction involves both electrons and phonons, there exist three primary types of thermal carrier interactions: electron-phonon coupling in metals, electron-phonon coupling at the interface, and phonon-phonon interaction at the interface, as shown in Fig. 9 (d) [176,177]. Consequently, the TBR at the interface resembles a network of R_{th} that needs to be calculated. On the metal side, heat transport involves both electrons and phonons, influenced by temperatures T_e and T_{ph} respectively. Conversely, on the non-metal side, heat conduction is primarily governed by phonons, characterized by temperature T_c. In the past period, researchers have conducted extensive research on the heat transport mechanism at the metal/semiconductor (metal/non-metal) interface [178–180]. Cheng et al. [178] conducted a comprehensive investigation of interfacial heat transport at epitaxial (111) Al/(0001) sapphire interface characterized by exceptionally high quality (atomically sharp, harmonically matched, and ultra-clean). It is found that elastic phonon scattering dominates the heat conduction at the Al-sapphire interface. Inelastic phonon scattering and electron-phonon coupling effects within the metal and at the interface were found to be negligible. Their analysis estimated that electron-phonon coupling contributes approximately 13.6 % to the total R_{th}. In a similar vein, Li et al. [179] studied the interfacial heat transport of two materials (Al/Si, Al/GaN) characterized by similar Debye temperatures, and found that a large part of phonons would be inelastic transferred on their interfaces at elevated temperatures, significantly improving the TBC. Furthermore, the study examines the correlation between interface quality and k_T, presenting distinct sharp and diffused interfaces as depicted in Fig. 10 (f). Figure.10 (g) illustrates the k_T predicted by MD at elevated temperatures. revealing that the TBC at the diffused interface is lower compared to that at the sharp interface. To provide further insight into the observed temperature-dependent thermal conductance, spectral phonon transmittance was calculated using the atomic green function, as illustrated in Fig. 10 (h). The sharpness of the interface critically influences phonon transport dynamics: atomically sharp interfaces facilitate inelastic phonon transport, whereas diffused interfaces hinder such transport. Notably, in practical GaN lateral device architectures, metallic contacts inherently form interfaces with the AlGaN layer. This configuration necessitates urgent investigation into the thermal transport properties at metal/AlGaN interfaces, as their characteristics critically influence device thermal and electrical performance. In related work, Miao et al. [180] simulated heat transport in metal/semiconductor multilayers and identified a critical thickness for the metal layer, as shown in Fig. 10(i) and (j). Beyond this critical thickness, electron-phonon coupling within the metal layer becomes significant in heat transport. Shi et al. [93] investigated the thermal transport characteristics at the β-Ga_2O_3/metal interface, emphasizing the pivotal role of the metal cutoff frequency in thermal conduction at the interface. At the metal cutoff frequency, heat transport does not increase further due to the elastic transport assumption. Interfaces between metals and semiconductors are prevalent in micro- and nano-electronics, where heat transfer mechanisms are complex due to diverse heat carriers involved. Further research is warranted to deepen our understanding of interfacial heat transport mechanisms.

4.2. Influence factors

Heat transport across micro-nano interfaces is intricately linked to the atomic properties of the materials flanking the interface, encompassing aspects such as bonding characteristics, crystal structure, defects, and applied pressure. These factors critically influence the coupling and scattering mechanisms of thermal carriers across the interface, including phenomena like phonon boundary scattering and phonon-electron coupling. The influencing factors and strengthening methods of interfacial heat transport are discussed in terms of interfacial coupling strength, bonding materials, lattice mismatches and defects. These considerations play crucial roles in determining the efficiency and effectiveness of heat transfer across such interfaces in various applications, including microelectronics and nanotechnology. Further exploration and optimization of these parameters are essential for advancing our understanding and improving the thermal management capabilities of micro-nano systems.

4.2.1. Interfacial coupling strength

The interfacial coupling strength between different materials plays a crucial role in determining interfacial heat transport [162]. This coupling strength is primarily governed by the type of interfacial bonding, which can be divided into van der Waals (vdW) force, hydrogen bond, covalent bond and metal bond [165]. vdW force represents the intermolecular interaction force, hydrogen bonds can occur both intramolecularly and intermolecularly, covalent bonds are strong intramolecular force, and metal bond entails the atomic force. In terms of strength, interfacial bonds rank from highest to lowest as follows: metal bond, covalent bond, hydrogen bond, and vdW force. In transistor applications, the interface connection mode is mainly vdW force and covalent bond (Fig. 11 (a)). The impact of interfacial coupling strength on heat transport across interfaces has been investigated extensively. Cheng et al. [181] achieved the integration of Ga_2O_3 thin films with diamond through vdW force, resulting in a TBC of 17−1.7/+2.0 MW/m^2·K (Fig. 11 (b)). Their study highlighted that the TBC between Ga_2O_3 and diamond is primarily influenced by three key factors: the relatively weak vdW bonding compared to stronger covalent bonds, the limited contact area at the interface, and a significant PDOS mismatch between Ga_2O_3 and diamond. Subsequently, Ga_2O_3 was deposited on the single crystal diamond substrate by ALD [182]. The TBC observed at this Ga_2O_3-diamond interface was approximately ten times higher than that achieved with vdW bonding (Fig. 11 (c)), underscoring the substantial impact of interface bonding on TBC. So et al. [183] investigated the interfacial heat transport of vdW heterostructures consisting of β-Ga_2O_3 and h-BN multilayers. After applying strain, the decrease of interfacial distance enhances the interaction between phonons and enhances the interfacial thermal conductance. These findings emphasize that interfacial coupling strength significantly affects thermal transport properties, with stronger bonding mechanisms leading to higher TBC.

4.2.2. Bonding-materials

The incorporation of a phonon spectrum intermediate layer and the introduction of nanostructures at heterogeneous interfaces are crucial strategies for reducing TBR [184–192]. Such bonding-materials serve as

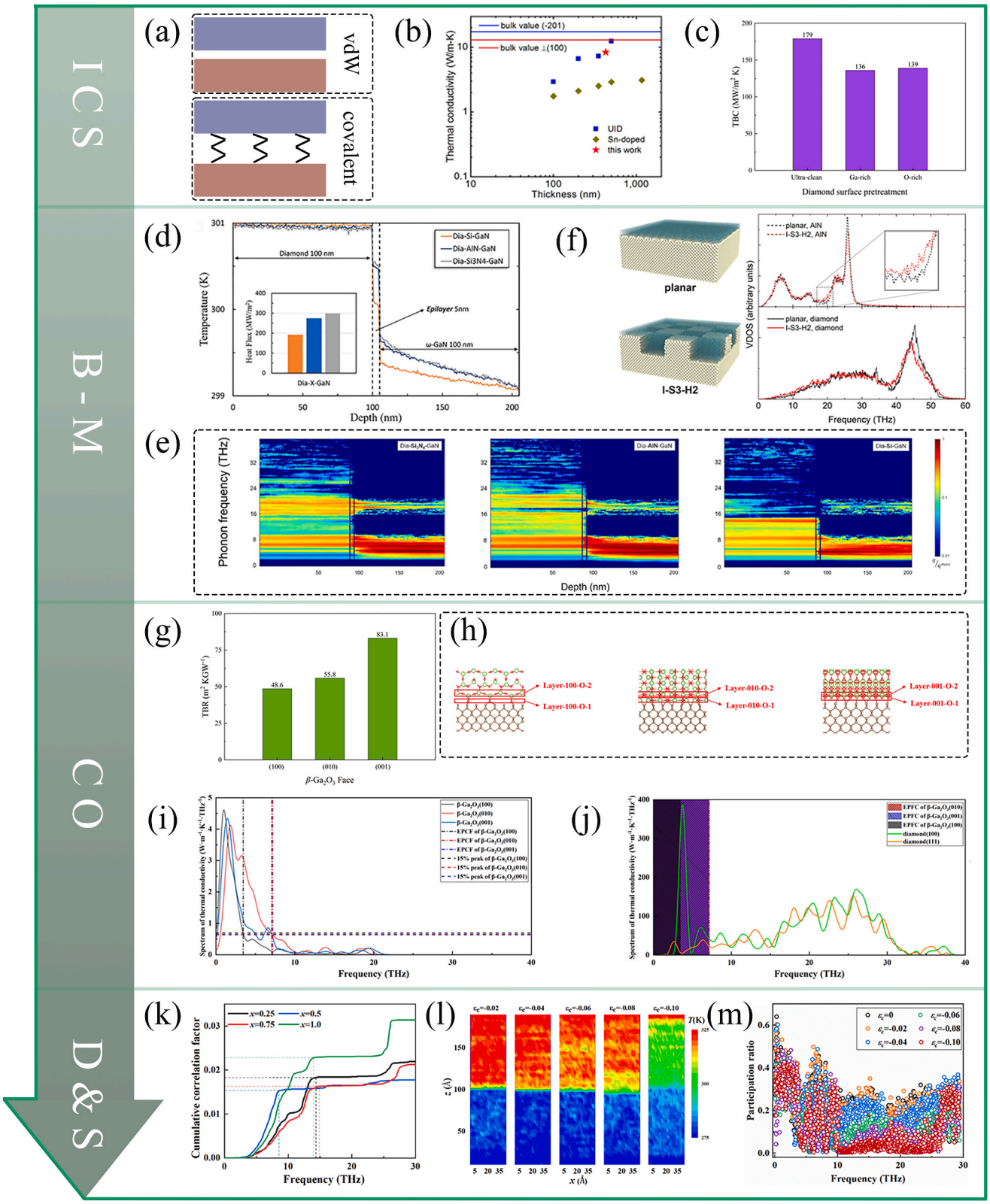

Fig. 11. (a) Diagram of vdW interface and covalent bond interface. (b) TBC of Ga_2O_3/diamond vdW interface [181]. (c) TBC of Ga_2O_3/diamond covalent bond interface [182]. (d) Temperature profiles and heat flux for various model interfaces with three different bonding-materials. (e) Comparison of the spectral heat flux of the three diamond-on-GaN models with different bonding-materials [187]. (f) Comparison of VDOS of AlN and diamond between planar interface and interface I-S3-H2 (nanopillars with size of 2 × 2 nm^2 and height of 3 nm) [192]. (g) TBR values across β-Ga_2O_3/diamond interfaces between different orientations of β-Ga_2O_3 [194]. O atom grouping diagrams (h) and thermal conductivity spectra (i) of β-Ga_2O_3 with different crystalline orientation. (j) Thermal conductivity spectra of diamonds with different crystalline orientation (*Copyright © 2024, American Chemical Society*) [175]. (k) Phonon cumulative correlation coefficients between GaN and $Al_xGa_{1-x}N$ on both sides of the interface. (l) Dependence of temperature distribution on compressive stress. (m) PPR on compressive strain [196]. (ICS: Interfacial coupling strength; B–M: Bonding-materials; CO: Crystal orientation; D&S: Doping and strain).

phonon bridges, enhancing phonon transmission coherence and thereby minimizing phonon interface scattering to reducing TBR. In the heteroepitaxial growth of semiconductors such as high quality GaN, nano-thickness transition layers are typically employed to mitigate lattice mismatch between the semiconductor and substrate materials. Despite the presence of defects within and near the interface of the transition layer material, which can somewhat hinder heat transport [174], phonon transport intermediates can be established between the semiconductor and the substrate materials to generally facilitate heat transfer across the interface. Cheng et al. [184] reported that GaN/-diamond interfaces with approximately 4 nm interlayers exhibit significantly higher TBC of about 50 MW/(m^2 K), the power density can reach 2.5 times higher than GaN-on-SiC and 5.4 times higher than GaN-on-Si. In their another study, Cheng et al. [185] utilized ion cutting and surface-activated bonding techniques to hetero-integrate wafer-level single crystal β-Ga_2O_3 films on a high k_T 4H−SiC substrate, employing an intermediate layer of Al_2O_3. Decreasing the thickness of the Al_2O_3 interlayer from 30 nm to 10 nm led to a 39 % increase in TBC values at the bonding interface and a 32 % increase at the annealed interface. Malakoutian et al. [186] found that 1 nm of SiN_x is converted to SiC during PCD growth, resulting in an exceptionally low TBR of about 3.1 ± 0.7 m^2 K/GW. Huang et al. [187] analyzed the TBR in in diamond/-GaN heterostructures with AlN, Si_3N_4 or Si coatings. In the absence of an intermediate layer, phonon propagation at the heterostructure interface is impeded due to the lack of a bridge to facilitate phonon transmission across the mismatched interface. Fig. 11 (d) presents a comparison of temperature distributions from diamond to GaN with various bonding-materials. It reveals that the diamond/Si/GaN configuration exhibits the most substantial temperature reduction and the lowest heat flux. Additionally, this configuration demonstrates the highest TBR among the three models. Fig. 11 (e) compares the spectral dependence of heat transport at the diamond/GaN using different bonding-materials. Brighter hot spots are observed in the Si_3N_4 bonding-material compared to AlN and Si, indicating that Si_3N_4 bridges the phonon band gap more effectively than AlN and Si. Gu et al. [188] for the first time explored heat transport at the Ga_2O_3-diamond interface containing an AlN buffer layer. Based on the first principles and pulsed laser deposition (PLD) technology, it is found that this strategy can effectively improve the quality of Ga_2O_3 films, including increasing crystallinity, surface smoothness and reducing oxygen vacancy. The TBC of the Ga_2O_3-diamond interface increased from 46.1 ± 2.3 MW/m·K to 60.9 ± 3.0 MW/m·K. In another study, Malakoutian et al. [189] explored various dielectric materials as buffer layers to create phonon Bridges at the GaN-diamond interfaces. Their research shows that the a-SiC buffer layer reduces the TBR of GaN-diamond (<5 m^2K/GW) by connecting low frequency and high frequency phonons.

Incorporating nanostructures at interfaces has been shown to significantly enhance heat transfer by increasing the effective contact area and optimizing atomic vibrations on both sides of nanopillar interfaces. Yang et al. [190] used atomic simulation methods to evaluate the changes of ITC under different Al-Ga atomic concentrations and interface roughness. As the interface roughness increases, the ITC decreases from 735.09 MW m^{-2} K^{-1} (smooth interface) to 469.47 MW m^{-2} K^{-1}, which is due to phonon localization caused by rough interface. Hua et al. [191] investigated the heat transport properties of nanostructures by phonon Monte Carlo technique. They identified that the enhancement of TBC is attributed to alterations in the heat conduction pathway induced by interfacial nanostructures. Furthermore, the enhancement in phonon transmission is facilitated by multiple interfacial reflections, which effectively scatter phonons and enhance their propagation across the interface. Qi et al. [192] studied the effect of nanopillar on the TBR of AlN/diamond interface using non-equilibrium molecular dynamics (NEMD) method, and found that the enhancement of AlN intermediate frequency phonons the movement of diamond vibrational density of states (VDOS) to low frequency are helpful to the optimization of interface thermal transport (Fig. 11 (f)). The TBR of the optimized nanopillar AlN/diamond interface is 28 % lower than that of the planar interface. In a related study, Qi et al. [193] utilized the NeuroEvolution Potential (NEP) approach to investigate the AlN/diamond interface and reached a similar conclusion. The micro-nano structure at the interface enhances material contact area and improves interatomic interactions.

4.2.3. Crystal orientation

Semiconductor materials like β-Ga_2O_3 exhibit anisotropic thermal properties, where these properties vary significantly across different lattice orientations. Consequently, the difference of crystal orientation at the interface greatly influences heat transport. Petkov et al. [194] investigated the TBR of β-Ga_2O_3 surfaces oriented along (100), (010), and (001) when bonded to vdW bonded diamond and ion-bonded amorphous Al_2O_3 interfaces (Fig. 11 (g)). Their findings reveal that TBR values at the vdW interface can vary by up to 70 % depending on the orientation of β-Ga_2O_3. In a related study, Sun et al. [175] studied the crystal orientation dependence and interfacial atom-dependent TBR of β-Ga_2O_3/diamond heterostructures after interfacial bonding using MD simulation of MLIP. The β-Ga_2O_3/diamond heterostructures with different interfacial atoms and crystal orientations are shown in Fig. 11 (h). They conducted a detailed analysis of the underlying heat transfer mechanism. Their study revealed that differences in the VDOS of β-Ga_2O_3 along different crystal directions significantly contribute to variations in TBR. Specifically, the orientation of β-Ga_2O_3 crystals affects how phonons interact at the interface, thereby influencing the overall TBR. The distribution of thermal conductivity and phonon frequency is depicted in Fig. 11(i) and (j). Depending on different diamond orientations, the TBR of β-Ga_2O_3/diamond interfaces is primarily influenced by the low-frequency phonons of diamond. The Effective Part Cutoff Frequency (EPCF) of β-Ga_2O_3(100) predominantly aligns with the first peak of diamond (111) and to a lesser extent with diamond (100). This characteristic results in a lower TBR for diamond (111) compared to diamond (100) when combined with β-Ga_2O_3 (100). Additionally, the choice of initial interatomic bonds between different atoms at the interface also influences the TBR. Specifically, when diamond is bonded with β-Ga_2O_3 (100), the initial Ga−C bonding configuration proves to be optimal. Conversely, when diamond interfaces with β-Ga_2O_3 (001), the O−C bond at the interface is preferred for enhancing thermal transport efficiency. These insights highlight the importance of crystal orientation in optimizing thermal transport properties across semiconductor heterostructures bonded to diamond interfaces.

4.2.4. Doping and strain

Doping engineering is a powerful method to alter both the electrical and thermal properties of materials. In semiconductor materials, there exists a significant relationship between doping and strain. During fabrication, strain at the interface is unavoidable due to lattice mismatch between the semiconductor material and the substrate, as well as differences in their coefficients of thermal expansion [195]. Chen et al. [196] studied the interfacial phonon information of GaN/$Al_xGa_{1-x}N$ heterostructures under the influence of ordered substitution doping and uniaxial compressive stress. Fig. 11 (k) illustrates the cumulative correlation factor up to the cutoff frequency, showing that the interfacial VDOS matching between GaN and AlN is much higher than that in the ternary-doped system. The introduction of Al atoms through doping increases phonon scattering at the heterojunction interface. Furthermore, the lattice vibration mismatch between Al and Ga atoms creates an uneven residual stress field at the interface, intensifying phonon interface scattering and promoting significant phonon localization. Under elastic strain, the heat transfer channel becomes more uniform with increasing strain (Fig. 11 (l)). Moreover, the PPR of interface phonons with respect to the compressive strain is illustrated in Fig. 11 (m). Moderate compression strain induces lattice distortions that enhance the overlap of interface phonon modes, and some local phonons play a role in the interface phonon transport, which optimizes the

interfacial phonon transport. Using full-scale molecular dynamics simulations, Yu et al. [197] explored that under 5 % external mechanical loading, the TBC of GaN/diamond heterostructures can achieve a 400 % change without damaging the interface, due to mechanical tunability of the interface morphology and phonon resonance. The research and optimization of interface thermal transport mechanisms have garnered increasing attention, particularly due to their crucial role in the thermal management of (U)WBG transistors [198–200].

5. Transistor design in transistor-level thermal management

In the realm of transistor-level thermal management, maintaining the essential electrical properties of transistors is paramount. This necessitates a synergistic approach known as thermo-electric co-design, which aims to maximize the heat dissipation capacity of transistors while preserving optimal electrical performance [6]. Enhancing electrical properties not only improves the operational efficiency of transistors but also has significant implications for thermal management. Through analysis of section.2 from a thermal perspective, by reducing heat generation and promoting the uniform distribution of Joule heating within the transistor, improved electrical performance helps mitigate the formation of hot spots. This approach also contributes to maintaining a uniform electric field, reducing the specific on-resistance $R_{on,sp}$, and enhancing switching characteristics. Therefore, optimizing electrical performance should be integral to transistor-level thermal management, with careful consideration of its impact on thermal field distribution. This section underscores the significance of transistor design in transistor-level thermal management, encompassing considerations of device architecture and junction terminal technology to achieve both efficient heat dissipation and optimal electrical functionality.

5.1. Device architecture

Over the years, the miniaturization of transistors has spurred the introduction of new materials and device architectures, such as SOI and FinFET, to meet evolving production and lifestyle requirements [201]. These advancements have substantially enhanced transistor electrical properties while also providing complementary improvements in thermal performance. Given the strong influence of transistor architecture on transistor-level thermal management, understanding its impact is crucial.

SiC MOSFET design research has been notably advanced [202–204], focusing extensively on achieving uniform E-field within the transistor. Earlier, Tan et al. [202] proposed a grooved gate SiC MOSFETs with P^+ shielding to mitigate E-field intensity within the grooved oxide layer, thereby facilitating lateral current diffusion into the drift region. The doping concentration of the current spreading layer (CSL) was increased relative to the drift region, effectively reducing the JFET resistance and significantly lowering $R_{on,sp.}$ Subsequently, grooved gate MOSFETs evolved into trench MOSFETs [203]. Duan et al. [204] propose a novel vertical double-diffused MOSFET, called Step high-*k* (Hk) vertical double-diffused metal-oxide semiconductor (VDMOS), aimed at enhancing E-field modulation effects and lowering $R_{on,sp}$. Another innovation is the 4H-SiC deep source trench MOSFET (DST-MOSFET) proposed by Na et al. [205]. The design described incorporates a P-pillar within the 4H-SiC deep source trench (DST) MOSFET structure, along with a side P+ shielding region (SPR) replacing the conventional gate trench bottom SPR. This configuration results in improved $R_{on,sp}$ and superior switching characteristics. SPR can effectively block the E-field concentration of gate oxide, thereby reducing E-field peaks. Madadi et al. [206] presents a Nanoscale SOI MOSFET with the Vertical Gaussian Doping Profile in Drain and Source regions (D-S-G-SOI) to improve the heating effects, aimed to decrease the E-field within the channel of the source and drain regions, crucial areas of the transistor. By reducing the E-field, it improves the potential distribution within the transistor, thereby mitigating temperature rise and addressing short-channel effects. As electronic devices operate at increasingly high frequencies, minimizing P_{sw} becomes critical as it directly impacts heat generation during operation. Zerroumda et al. [207] propose a high-performance 4H-SiC trench power MOSFET incorporating the junction-less (JL) concept. This innovative design merges the advantages of JL technology with gate trench-based MOSFET architecture. An important consideration is the trade-off between P_{loss} and switching characteristics, as reducing $R_{on,sp}$ can potentially impact transistor switching performance. It demonstrates that the transistor maintains low C_{iss} values across a wide range of drain operating voltages, which enhances gate switching speed. This improvement primarily stems from the role of JL technology in reducing gate capacitance. Sun et al. [208] proposed and studied a SiC trench MOSFET with integrated auto-adjust source-potential region (AS-TMOS), which incorporates a lightly doped P base and a heavily doped P shield around a stepped thick oxide gate groove. The deeper source-potential region in AS-TMOS can effectively limit the E-field in the gate oxide (Fig. 12 (a)). Compared to conventional trench MOSFETs (C-TMOS), AS-TMOS demonstrates reduced surge voltage and turn-off P_{sw}, particularly under conditions of stray inductance (L_s) of 10 nH, as shown in Fig. 12 (b). Furthermore, AS-TMOS effectively mitigates switching oscillations and minimizes P_{sw}, thereby lowering peak T_j by 200K, as depicted in Fig. 12 (c). In another approach, Song et al. [209] propose a new method of co-regulation of gate and channel currents based on gate charge compensation, which can reduce the on-off loss by up to 81 %.

In recent years, advancements in Gallium Nitride (GaN) transistor research have led to the development of various designs catering to diverse applications, including current aperture vertical electron transistors [210], channel MOSFETs [211], and power FinFETs [212]. These designs aim to enhance both electrical and thermal performance crucial for modern electronics. Wang et al. [213] conducted a study focusing on the thermal performance of vertical GaN FinFETs and proposed three innovative designs: reduced fin spacing, oxide full fill (FF) and split grid (SG) structures. The primary objective of reducing fin spacing and employing oxide FF structures is to minimize dielectric parasitic capacitance, thereby improving overall transistor performance. The SG structure takes a different approach by eliminating gate metal in the interface zone, which exposes the drift layer to the source metal field. This design modification enhances switching performance coefficients by 58 % and reduces P_{sw} by 38 %. Furthermore, adjustments in cell spacing and array aspect ratios have been shown to significantly lower peak temperatures within the cell array [214]. The researchers have alleviated E-field congestion at the structural level and reduced $R_{on,sp}$ [215–218]. Ghaffari et al. [215] introduced a groove structure in GaN transistors located between the buffer layer and nucleation layer. This structural modification increased the BV of the transistor by 56 %. Wei et al. [216] identified strong channel-to-channel coupling as a critical factor in reducing the $R_{on,sp}$ of double-channel-MOS-HEMT. In another study, by inserting an avalanche diode into the buffer layer of an enhanced GaN HEMT, the gate-drain E-field distribution can be improved [217]. Miyamoto et al. [219] improved the E-field distribution in the channel by forming a high layer of potassium film between the drain and gate of a GaN HEMT and modulating the film thickness in the transverse direction. Shen et al. [220] proposed an enhanced mode (E-mode) p-GaN gate AlGaN/GaN HEMT based on novel strain technology (NST), as shown in Fig. 12 (d). NST involves GaN/AlGaN/GaN and AlN/AlGaN/GaN heterojunctions extending from the gate to the drain side. This innovative design introduces an additional E-field peak away from the gate edge, thereby reducing the peak E-field around the gate region, as illustrated in Fig. 12 (e). This approach improves device reliability and efficiency by minimizing E-field-induced effects that can affect performance and longevity.

Ga_2O_3-based transistors are emerging as highly promising devices currently under active development. Zhou et al. [221] proposed a Variation of Lateral Doping (VLD) technique targeted at reducing the

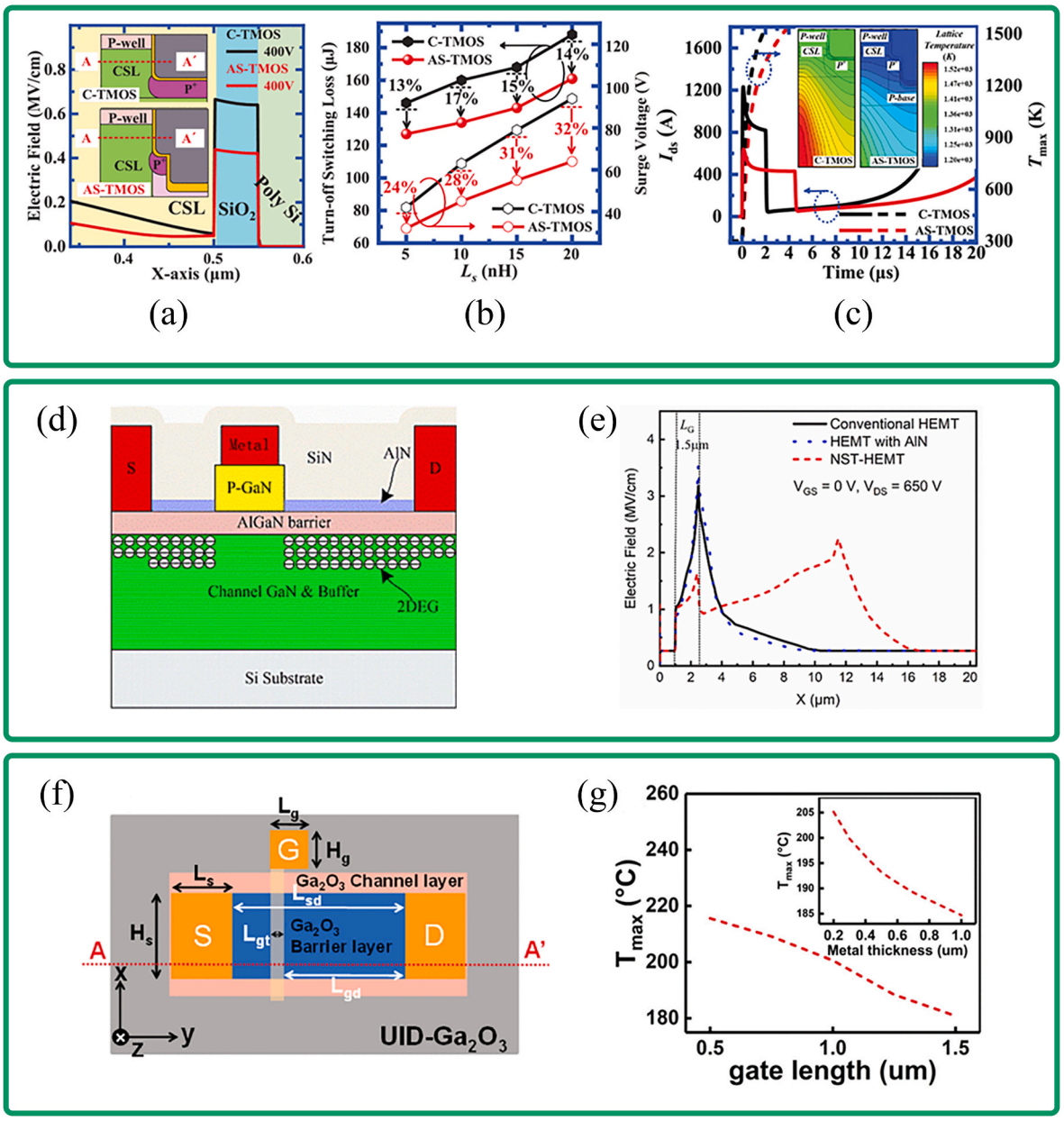

Fig. 12. (a) Lightly doped P-base thickness (t_{pb}) dependence of the gate-end electric flux of AS-TMOS. The inset is the E-field distribution of both TMOS. (b) Surge voltage and turn-off switching loss for both TMOS. (c) Electro-thermal simulation of SiC AS-TMOS and C-TMOS under 800V short circuit condition (*Copyright © 2023, IEEE*) [208]. (d) The cross-sectional schematic of NST-HEMT. (e) Simulated electric field distributions along channel biased at off-state (VGS = 0 V, VDS = 650 V) [220]. (f) Schematic of the investigated single finger MESFET. (g) T_{max} as a function of gate length (from 0.5 to 1.5 μm). Inset: T_{max} as a function of the thickness (from 0.2 to 1 μm) of all the metals (S, D, and G) ((*Copyright © 2023, IEEE*)) [94].

off-state E-field within the channel. In Ga_2O_3 FinFETs, increasing the fin width (W_{fin}) has been identified as a critical parameter influencing the $R_{on,sp}$ and thereby affecting the T_j. Increasing W_{fin} has been demonstrated to decrease $R_{on,sp}$, which in turn lowers T_j. Conversely, increasing the spacing between fins (S) results in higher $R_{on,sp}$ and occupies more space within the transistor, potentially impacting T_j negatively [133]. Previous studies have shown that the channel direction, the distance between gate and drain metal electrodes, the geometry of the interconnect connecting metal electrodes and bonding pads play an important role in the heat dissipation of the active region of the transistor. Kim et al. [222] investigated the effect of the distance between gate and drain metal electrodes on the thermal performance of β-Ga_2O_3 MOSFETs. They observed that MOSFETs with different gate-drain distances (L_{GD} = 1 μm, 6 μm, and 11 μm) exhibited similar electrical behavior due to their equivalent effective electronic channel lengths. However, when comparing thermal performance, they found that reducing the lateral distance between the gate and drain metal electrodes from 11 μm to 1 μm resulted in a significant reduction in gate temperature rise by 25 %. Xie et al. [223] optimized β-Ga_2O_3 SBD electrode designs on SiC using 3-D Raman thermometry and electrothermal simulations. Their results demonstrate that enlarged electrode gaps and chamfered edges improve heat dissipation while preserving electrical performance (I_{ON}/I_{OFF} ratio, subthreshold swing, ideality factor, and on-resistance). Figure.12 (f) illustrates the schematic of the investigated single finger MESFET by Mao et al. [94]. Through increasing the gate length from 0.5 μm to 1.5 μm was found to lower the maximum channel temperature by 35 K, as shown in Fig. 12 (g), equivalent to optimizing the substrate k_T of the transistor from 100 W/m K to 2000 W/m K. In addition, the T_{jmax} difference is about 60 K when the gate length is aligned with the direction of the highest and lowest in-plane k_T of β-Ga_2O_3. This highlights the

importance of strategically designing the layout on the three-dimensional anisotropic β-Ga_2O_3 substrate to enhance heat dissipation capabilities. These findings highlight the critical role of layout optimization in mitigating hotspots and improving thermal management in β-Ga_2O_3 transistors, crucial for enhancing device reliability and performance in practical applications.

Multifinger device architectures are widely utilized in power and radio-frequency (RF) applications to facilitate high-current operation. However, thermal crosstalk between adjacent gate fingers exacerbates localized heat accumulation, leading to substantial degradation in both electrical performance and long-term device reliability. To overcome this challenge, optimized layout designs are essential for effective thermal mitigation. A. Manoi et al. [224] investigated transient thermal crosstalk in multifinger AlGaN/GaN HEMTs using time-resolved Raman thermography, revealing its time-dependent nature. Their findings demonstrate negligible thermal crosstalk between device fingers within the first 500 ns of operation. However, beyond this threshold, significant thermal interaction emerges, particularly in devices with gate pitches below 40 μm. Further elucidating this phenomenon, J. Jeong et al. [225] demonstrated that thermal crosstalk contributes substantially to heat generation in multi-finger GaN-on-Si HEMTs, accounting for up to 60 % of the thermal load in central fingers. To mitigate these effects, they proposed a non-uniform multi-finger layout design that effectively redistributes heat and reduces thermal crosstalk. This approach resulted in decreased temperature variation among fingers, along with alleviated subthreshold swing and ON-current degradation, indicating enhanced device reliability. In a complementary study, Shoemaker et al. [226] design a vertebrae-shaped multi-finger α-Ga_2O_3 device layout via device thermal characterization and modeling that mitigates thermal crosstalk by decentralizing the overall device heat generation profile. Given its substantial impact on thermal performance, thermal crosstalk in multi-finger devices warrants thorough investigation to advance next-generation high-power and RF electronics.

5.2. Junction terminating techniques

Junction technology in power transistors is crucial for managing electrical field intensities, mitigating edge effects of the E-field, and ensuring uniform redistribution of joule heat. Various junction termination techniques are employed across different transistor configurations to achieve these objectives. In vertical transistors, common junction termination techniques include field plate (FP) [227,228], field limiting ring (FLR) [229,230], junction termination extension (JTE) [231] and inclined surface termination [232]. In lateral transistors, techniques such as inlet plate technology [233], polarized super-junction technology [234], RESURF technology [235] and doping compensation technology [236]. Each of these junction termination techniques is designed to optimize the E-field distribution, reduce E-field gradients, and enhance overall transistor performance and reliability in power applications.

Several scholars have investigated the impact of junction terminal technology on the thermal characteristics of transistors. Šodan et al. [237] initially highlighted the significance of FP design in enhancing the thermal performance and reliability of transistors. They demonstrated that integrating FPs to reduce $R_{th,j\text{-}c}$ can significantly lower T_j, which is a critical consideration in early-stage design phases. In a related study, Qu et al. [238] systematically studied the effects of NCD FPs on both electrical and thermal characteristics of Ga_2O_3 MOSFET using

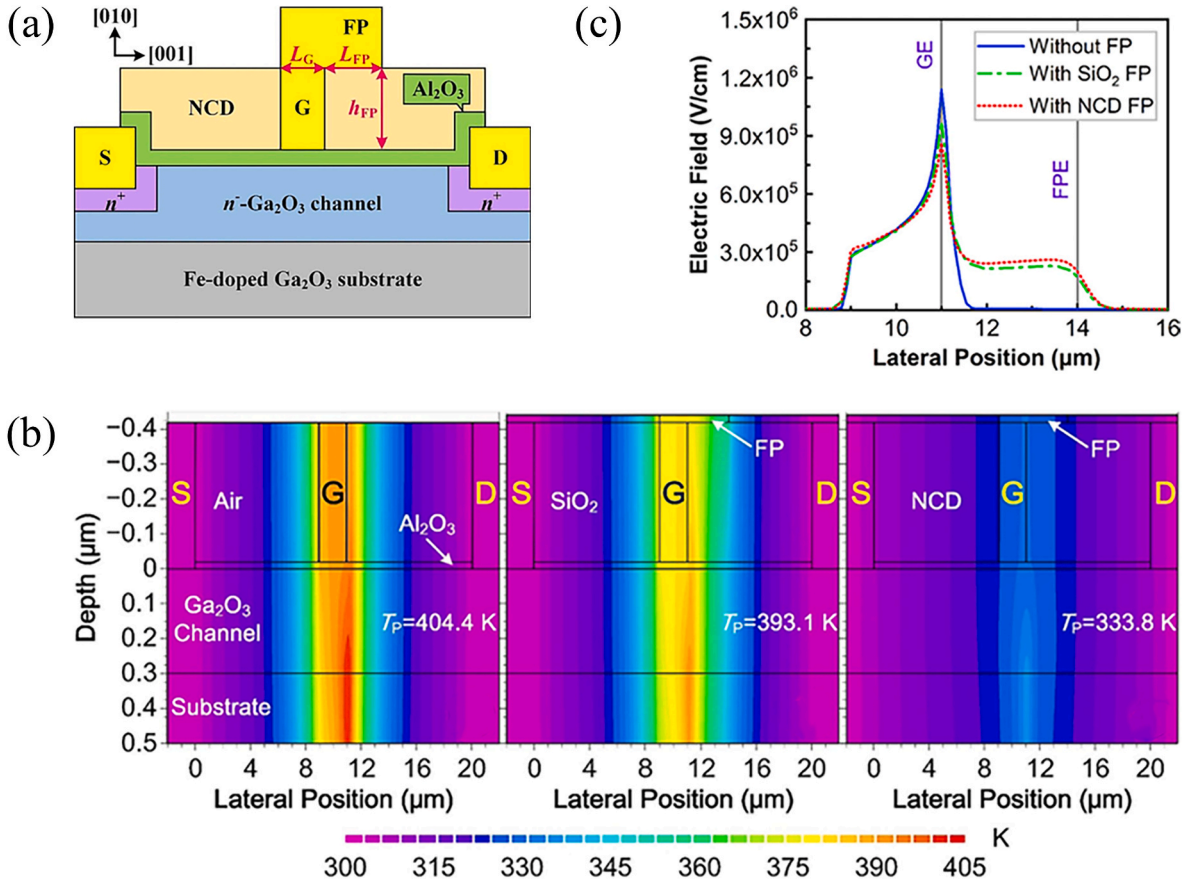

Fig. 13. (a) Cross-sectional schematic of the Ga_2O_3 MOSFET with the NCD gate FP. (b) Temperature distributions of Ga_2O_3 MOSFETs with the power dissipation density of P = 1.4 W/mm at V_{GS} = 4 V. From left to right are non-field-plated devices, SiO_2 field-plated devices, and NCD field-plated devices. (c) Electric field distributions along the channel for Ga_2O_3 MOSFETs with different structures at V_{GS} = 4 V with the power dissipation density of P = 1.4 W/mm [238].

electrothermal device simulation. Figure.13 (a) illustrates the schematic of the Ga_2O_3 MOSFET with the NCD gate FP. According to the temperature distributions shown in Fig. 13 (b), for devices operating at power density of P = 1.4 W/mm, the maximum temperature rise of the device could be reduced by more than 67 % through the implementation of NCD FPs. The observed reduction in temperature rise is attributed to the lower peak E-field intensity near the drain side channel and beneath the gate edge in Ga_2O_3 MOSFETs equipped with NCD FPs compared to those with SiO_2 and field-free plate structures (Fig. 13(c)). A concentrated local E-field accelerates electrons at the gate drain edge, leading to intense phonon scattering and significant heat generation in that region. Han et al. [239] proposed a novel tapered doping tail modulated junction termination extension (TDTM-JTE) technique, in which the peak E-field is well suppressed. The curvature of the edge of the p + n junction is eliminated, resulting in E-field remodeling in the JTE region. Research indicates that employing an E-field plate can achieve two beneficial outcomes: it adjusts the E-field distribution to a more uniform profile and reduces the E-field intensity at the gate edge. Consequently, this mitigates scattering between phonons and between phonons and electrons within the channel, thereby contributing to a reduction in T_j. As previously discussed, from a thermal perspective, mitigating E-field crowding facilitates a homogeneous distribution of joule heat within the transistor, thereby minimizing thermal hot spots.

The primary objective of transistor design is to achieve uniform E-field distribution, minimize $R_{on,sp}$, and enhance switching characteristics. While these efforts primarily target electrical performance, they inevitably yield positive implications for thermal performance as well. Consequently, optimizing electrical properties must be considered within the framework of transistor-level thermal management, with careful attention to its impact on thermal field distribution. This integrated approach ensures that both electrical performance and thermal dissipation are effectively balanced to enhance overall device reliability and performance.

6. Challenges and perspectives

6.1. Interface thermal transport characteristics

At present, the research of interface thermal transport mechanism mainly relies on simulation technology to further explore. Although methods such as MD are able to accurately calculate the TBR values of complex practical material systems that take into account the interface structure at the atomic level, they fail to provide a physical basis for the underlying scattering mechanism at the interface. The understanding of phonon-phonon coupling and electron-phonon coupling mechanisms at interfaces remains controversial due to a lack of definitive experimental evidence. Further experimental studies are necessary to elucidate these mechanisms. The phonon model proposed for interfaces, initially predicted in the last century, purportedly exists within a few atomic layers near the interface. However, direct experimental observation and measurement of its spatial distribution and dispersion relationship have not yet been achieved.

The energy of interface phonons is contingent upon both spatial coordinates and momentum. Detecting phonon dispersion at interfaces necessitates experimental techniques capable of achieving nanometer or even atomic-level spatial resolution and momentum resolution within the first Brillouin zone (10^{-9} m). Additionally, high detection sensitivity and energy resolution are essential for accurate measurement. Qi et al. [240] used four-dimensional electron energy-loss spectroscopy (4D EELS) technique to observe interface phonons at the crystal heterojunction interface, marking the initial experimental detection of their existence. The schematic of 4D EELS is illustrated in Fig. 14 (a). They measured the spatial distribution, local density of states, and dispersion relationships of these phonons, as illustrated in the accompanying Fig. 14 (b) and (d), demonstrating good agreement with calculations (Fig. 14(c) and (e)). In a related study, Li et al. [241] used 4D EELS technique to measure phonon patterns at the interfaces of AlN/Si and AlN/Al. Their research delved into phonon transport behaviors across different interfaces and assessed the role of interface phonons in thermal conductivity. This innovative approach significantly enhances the comprehension of interface phonon transport and heat transfer dynamics at an experimental level.

Furthermore, the utilization of machine learning technology in interface thermal transport and bonding material design is expanding, but the challenge is the scarcity of experimental TBR data across diverse materials. Therefore, it is imperative for future research to establish comprehensive and precise databases at the experimental level that encompass interface-related characteristics. Such databases are essential to facilitate the application of machine learning in understanding interface thermal transport properties and optimizing TIM design. Ultimately, this advancement will enhance promote the interface thermal transport process in transistor-level thermal management.

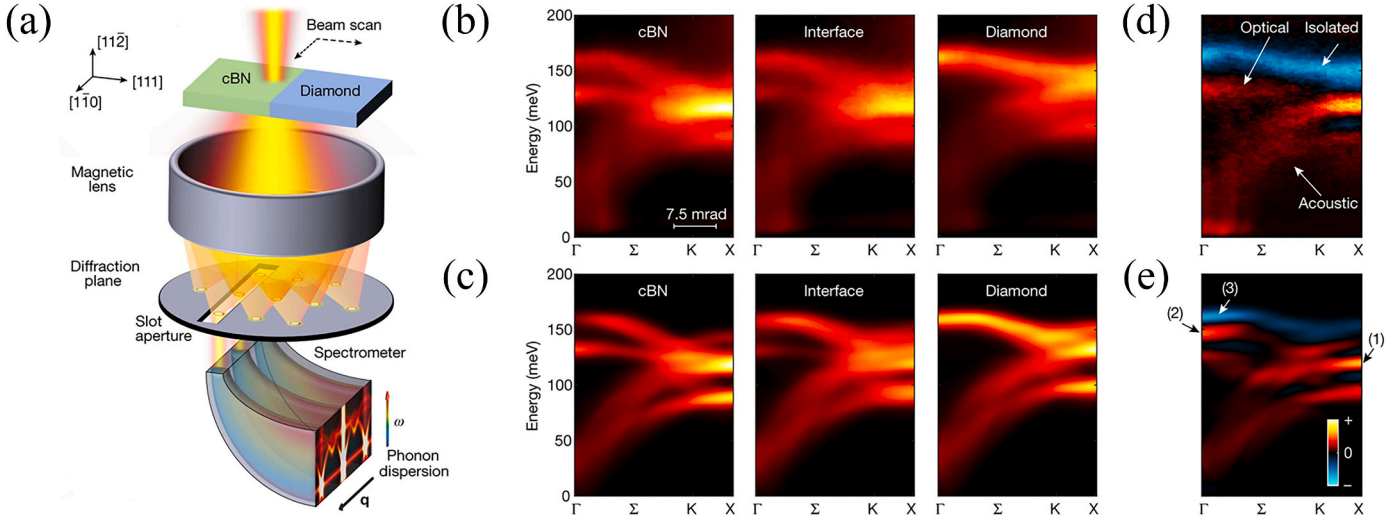

Fig. 14. (a) The schematic of the experimental setup (4D EELS) used to acquire phonon dispersion curves. The measured phonon dispersion diagrams (b) and the corresponding simulation results based on DFPT (c) calculations along the Γ–Σ–K–X line with the beam located in c-BN (left), at the interface (middle) and in diamond (right). The measured (d) and calculated (e) difference between the interface spectra and the average of two bulk spectra [240].

6.2. Thermal transistor

With the increasing integration of semiconductor power electronics, the power density is increasing. This heightened density leads to localized high heat fluxes during operation. Failure to promptly dissipate this heat poses substantial risks to electronic safety and stability. While traditional heat spreaders passively conduct heat away from hot spots, there remains a notable absence of more dynamic methods to actively regulate heat transfer. Recently, a lot of work has been done on dynamic based thermal management methods [242–247]. However, these approaches typically rely on phase transitions, mass transfer, fluid dynamics, and similar mechanisms to regulate heat transport capacity. A significant limitation of these methods is their response speed, typically ranging from minutes to hours (well below 1 Hz). In contrast, a thermal transistor represents a novel concept where the k_T can be dynamically modulated in real-time by external stimuli. This capability holds immense potential for transformative applications in dynamic thermal management, energy harvesting, and phonon logic.

Li et al. [248] have pioneered the development of a groundbreaking solid-state thermal transistor that demonstrates exceptional performance at room temperature. The device channel connects to hot and cold reservoirs maintained at temperatures T_H and T_C, respectively. The third terminal, analogous to a gate in electronic transistors, controls the k_T of the channel and thereby regulates heat flow. The operational principle of this thermal switch hinges on electrically modulating the atomic bond strength within the molecular junction, thereby controlling k_T. Their device boasts a switching speed exceeding 1 mHz, a switching ratio surpassing 1300 %, and reversibility over 1 million gated cycles, as depicted in Fig. 15(b) and (c). A symbolic diagram akin to an electronic transistor in Figure.15 (a) illustrates the concept of this thermal switch. This innovative approach enables faster and more precise manipulation of heat flow, and is expected to be the pinnacle of thermal management technology.

6.3. Advanced heterogeneous integration technology

Heterogeneous integration technology has emerged as a critical enabler for advanced transistor-level thermal management, facilitating the development of high-performance power devices with enhanced heat dissipation characteristics. The establishment of high-quality heterojunctions constitutes a fundamental requirement for efficient thermal transport, as interfaces exhibiting low defect densities and strong phonon coupling demonstrate substantially reduced TBR. Currently, two primary methodologies dominate heterogeneous integration approaches: wafer bonding and epitaxial growth techniques.

Wafer bonding comprises two main approaches: (1) direct bonding (including fusion bonding, low-temperature plasma activation bonding, room-temperature surface activation bonding, and anodic bonding) and (2) indirect bonding (encompassing metal-thermal compression bonding, eutectic bonding, solid-liquid interdiffusion/transient liquid phase bonding, adhesive bonding, and glass frit bonding) [249]. For the recent state-of-the-art β-Ga_2O_3-diamond MOSFETs by wafer bonding, Zhao et al. [250] pioneered wafer-scale β-Ga_2O_3 single-crystal arrays on diamond via transfer printing. The β-Ga_2O_3-on-diamond RF MOSFETs achieves record performance: 810 mA/mm on-state current, 61 GHz f_{max} (pre-de-embedding), and ultra-low R_{th} (5.52 K mm/W).

Conventional epitaxial growth techniques include metalorganic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), low-pressure chemical vapor deposition (LPCVD), and hydride vapor phase epitaxy (HVPE). For Ga_2O_3 epitaxy, Mist chemical vapor deposition (Mist-CVD) has emerged as an attractive alternative, offering distinct advantages including: low-cost, non-vacuum, and simple-to-operate. Li et al. [251] integrate theories of microchannel heat and mass transfer with crystal growth principles to establish the correlations between the mist morphology and the 2D-3D crystal growth of α-Ga_2O_3 films have been established. High-quality α-Ga_2O_3 film fabrication has been realized with full width at half maxima (FWHM) of 37 arcsec, root

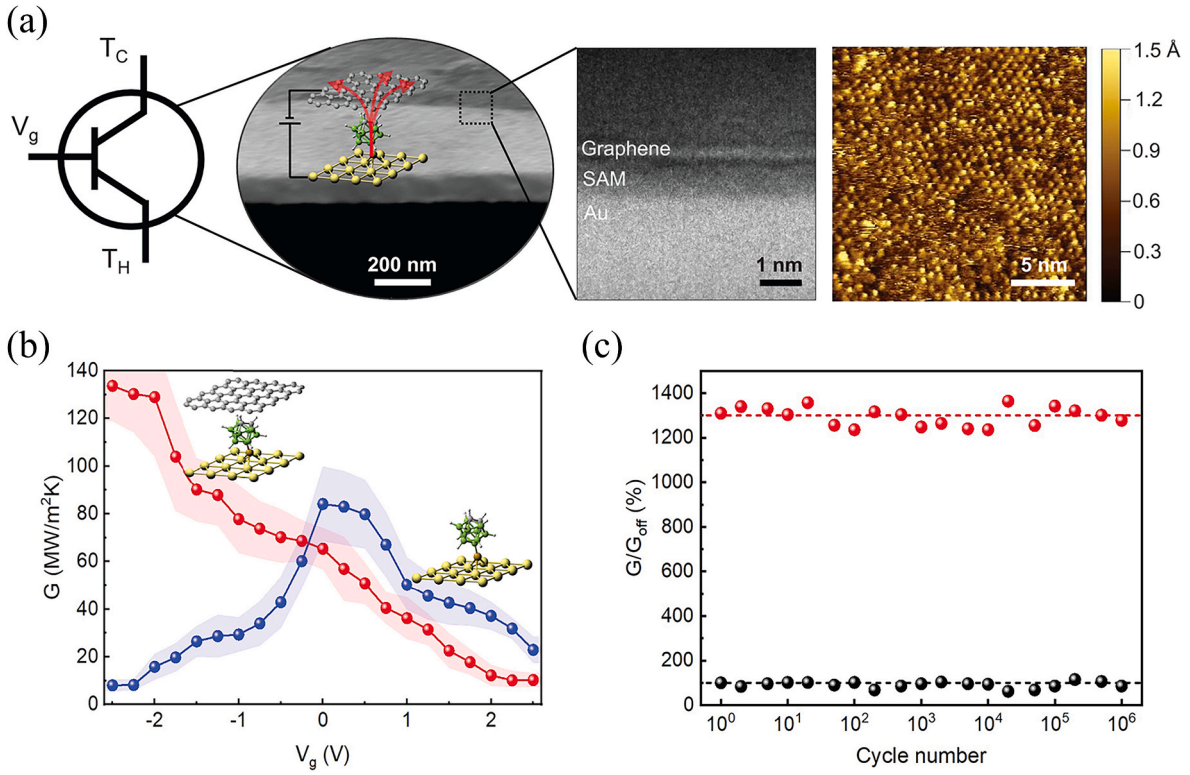

Fig. 15. (a) Conceptual illustration and structure of the three-terminal thermal device. (b) The measured thermal conductance (G) as a function of gate voltage (Vg). (c) Reversibility test of electrical gating between ± 2.5 V on cycling measurements of the thermal device with graphene up to 1 million times. The value of G_{off} is 10 MW/m^{2}K [248].

mean square (RMS) of 1.66 nm, and optical bandgap (E_g) of 5.32 eV. Yan et al. [252] demonstrated high-quality β-Ga_2O_3 growth on NiO buffer layers via Mist-CVD, achieving excellent crystallinity (FWHM: 0.514°) and surface smoothness (RMS: 3.34 nm) with minimal micro-strain. While these results are promising, comprehensive characterization of interfacial thermal transport properties remains essential to fully evaluate this technique's potential for power electronics applications.

By leveraging high-quality heterostructures, future power electronics can achieve unprecedented power densities while maintaining operational stability, underscoring the critical role of heterogeneous integration in next-generation thermal management strategies.

7. Conclusion

The rapid advancement of power electronics, driven by (U)WBG semiconductors, has enabled unprecedented improvements in efficiency and power density. However, these benefits are accompanied by significant thermal management challenges arising from high-power densities and device miniaturization, particularly at the transistor level where localized hotspots can severely compromise performance and reliability. This review provides a comprehensive analysis of transistor-level thermal management strategies, focusing on two critical aspects: (1) reduction of $R_{th,j\text{-}c}$ and (2) optimization of P_{loss}.

1 Transistor-level thermal management on reducing $R_{th,j\text{-}c}$:

1.1 Side-Cooling Methods:

Junction-side cooling (e.g., diamond passivation, 2D material radiators, flip-chip integration) excels in extracting heat directly from hotspots.

Bottom-side cooling (e.g., high k_T substrates like SiC, diamond, and BAs; embedded microchannels) leverages larger substrate areas for efficient heat dissipation.

Double-side cooling combines the strengths of both approaches, achieving the lowest R_{th} values.

While these methods effectively reduce thermal resistance, their implementation faces challenges in achieving high-quality interfacial integration. Advances in manufacturing processes, including wafer bonding, epitaxial growth, deposition, and etching technologies, are critical for further development. Crucially, these thermal solutions must be implemented without compromising the structural integrity of semiconductor materials.

1.2 Interface Thermal Transport:

The TBR at material interfaces remains a significant bottleneck. Strategies such as interfacial coupling strength, bonding-materials, crystal orientation, and doping and strain have shown promise in reducing TBR.

However, significant discrepancies persist between simulated and experimental results. Emerging techniques such as MLIPs and advanced characterization methods (e.g., 4D EELS) are enabling more accurate modeling and deeper understanding of interfacial thermal transport phenomena.

2 Transistor-level thermal management optimizing P_{loss}:

Thermo-electric co-design is essential for balancing electrical performance and thermal management. Transistor architecture and junction terminal technologies that effectively homogenize E-fields, reduce $R_{on,sp}$, and optimize switching characteristics, which can not only enhance efficiency but also mitigate self-heating effect. Multifinger device architectures, while enabling high-current operation, require careful layout optimization to minimize thermal crosstalk.

These design approaches intrinsically homogenize heat generation and reduce hotspot temperatures, offering advantages that are less constrained by fabrication limitations. However, as power densities continue to increase, synergistic integration with thermal resistance reduction strategies becomes essential.

Future research should prioritize.

1. To optimize device performance, a thermo-electric co-design approach must be adopted, integrating thermal management with electrical performance considerations. Semiconductor materials and their interfacial thermal properties should be systematically investigated and enhanced to elucidate how improved thermal characteristics contribute to electrical performance. Furthermore, in proposed device optimization strategy, comprehensive thermal distribution analysis should be conducted to ensure balanced performance.
2. Exploration and Breakthrough of Integrated Interfaces. Future research should focus on advancing integrated interface technologies by optimizing wafer bonding and epitaxial growth processes, elucidating the fundamental mechanisms governing interfacial thermal transport through phonon scattering and strain effects, and bridging the gap between simulation and experiment by leveraging machine learning-assisted molecular dynamics alongside advanced characterization techniques like 4D EELS, TDTR and 3-Ω, thereby enabling precise control of interfacial thermal resistance for next-generation ultra-wide bandgap power electronics. By addressing these challenges, next-generation (U)WBG power devices can attain exceptional power densities and reliability, fully realizing their potential for high-performance electronics. This review, grounded in the principles of electro-thermal co-design, emphasizes the crucial role of interdisciplinary collaboration across materials science, microelectronics, thermal engineering, and computational physics in advancing transistor-level thermal management solutions, thereby enabling sustainable progress in power electronics technology.

CRediT authorship contribution statement

Guangzheng Zhang: Writing – original draft, Investigation, Conceptualization. **Shilin Dong:** Writing – review & editing, Formal analysis. **Qian Xin:** Supervision, Writing – review & editing. **Lin Guo:** Writing – review & editing, Project administration, Funding acquisition. **Xinyu Wang:** Supervision, Formal analysis. **Gongming Xin:** Supervision, Resources, Funding acquisition. **Ning Qin:** Supervision, Investigation, Funding acquisition. **Xin Lan:** Methodology, Investigation. **Chunsheng Guo:** Methodology, Data curation. **Wei Wang:** Methodology. **Bing-yang Cao:** Supervision, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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